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m-Mode SVPWM Technique for Power Converters

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Preface

In traditional SVPWM, all operating modes or voltage space vectors of the inverter need participate in modulation, which results in a large amount of calculation in the digital processor and the corresponding computational complexity. It is well known that reducing the number of voltage space vectors is a potential methodology to simplify the calculation of SVPWM.

Since 2001, the authors have studied the modulation characteristics of power electronic converters to solve the computational complexity problem of SVPWM. In terms of the system state controllability, it is found that not all voltage space vectors are required for the SVPWM process, when the inverter is regarded as a switched linear system. Further, some redundant voltage space vectors can be ignored to reduce the computational complexity of SVPWM and achieve the desired control output. Based on the above results, the rotating voltage space vector can be synthesized by fewer voltage space vectors, and a novel and simpler SVPWM can be obtained. In fact, any rotating voltage space vector has a variety of synthesis methods on the basis of the space vector graph of SVPWM, when the angle between two voltage space vectors forming the rotating voltage space vector is less than 180°, so it is possible to choose the modulation method having fewer voltage space vectors to realize SVPWM. The drawn conclusion of the system state controllability analysis in geometry can be confirmed.

Therefore, in view of the system state controllability, the authors do propose the mechanism and criterion of *m*-mode SVPWM, and develop the corresponding strategies applied for two-level inverters, dual-output inverters, multiphase inverters, three-level inverters, modular multilevel inverters, and PWM rectifiers. Theoretical and experimental results validate that *m*-mode SVPWM has simpler calculation, lower switching frequency, and higher efficiency than the existing SVPWM. The *m*-mode SVPWM, we concluded, is an innovative one.

This book consists of four parts. According to the switched linear system theory, the first part reveals the state controllability of power electronic converters and puts forward the corresponding *m*-mode state controllability criteria and the *m*-mode SVPWM mechanism. Based on the above theory, the *m*-mode SVPWM strategies of the three-phase four-wire inverter, nine-switch dual-output inverter, five-leg

dual-output inverter, and three-phase three-level inverter are proposed in the second part in detail, and the proposed SVPWMs are compared with the traditional ones to verify their superiorities. By reducing the number of inverter operating modes, the following part exhibits the application of *m*-mode state controllability to the complex modular multilevel inverter to simplify the PWM strategy. The *m*-mode SVPWM mechanism, in the last part, is popularized and applied to the PWM rectifier.

And, withal, an inspiration is given from this book: multi-interdisciplinary research can achieve novel outcomes. For example, considering power electronic converter only from the circuit theory, the factors that promote the development of power electronic technology show less vitality. Switched linear system theory, however, draws new elicitation for the study of power electronic converters. It is even possible to achieve further discoveries, tap the potentials, and take full advantage of the new characteristics of power electronic converters. Therefore, it is interdisciplinary that enlightens the future direction in research of power electronics technology.

Guangzhou, China Bo Zhang
October 2018 Dongyuan Qiu

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Chapter 1
Introduction

1.1 Review of PWM Converter

Pulse-width modulation (PWM) is one of the core technologies of power electronic converters and it was initially proposed to allow inverters to output sinusoidal AC voltage and current. Up to now, it has been applied to the AC–AC matrix converters and PWM rectifiers. Although PWM has been proposed for nearly 60 years since 1964, due to the continuous emergence of various new power electronic converters and the increasing requirements for the quality of converters' output voltage and current, PWM is still one of the most popular research directions in the field of power electronics, and continues to attract attention and interest of researchers.

PWM methods are usually divided into sinusoidal pulse-width modulation (SPWM) and space vector pulse-width modulation (SVPWM) according to the principle of generation. For inverters, there are three main indicators to evaluate the performance of PWM method: (1) Harmonic content; (2) Utilization of the DC voltage; and (3) Switching times. Besides, with the development of PWM method, it is necessary to consider the difficulty of the control method implementation, the possibility of soft switching, and the ability to suppress common mode (CM) and differential mode (DM) interferences simultaneously.

The analysis of the inverters' harmonic content is mainly based on the Fourier series method [1]. Assuming that the output voltage v of the inverter is a function of the period T, its root mean square (RMS) value is defined as

$$V_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T v^2 \mathrm{d}t} \tag{1.1}$$

Since the voltage signal v is periodic, it can be expressed by the Fourier series as follows:

$$v = V_1 \cos \omega t + V_2 \cos 2\omega t + V_3 \cos 3\omega t + \cdots, \tag{1.2}$$

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where $\omega = 2\pi/T = 2\pi f$, V_n $(n = 1, 2, 3, \ldots)$ is the amplitude of the component at frequency $f_n = nf$.

Thus,

$$V_{\text{rms}} = \sqrt{\frac{1}{T}\int_0^T \sum_{n=1}^{\infty}\sum_{k=1}^{\infty} V_n V_k \cos n\omega t \cos k\omega t \,\mathrm{d}t} \tag{1.3}$$

The integral term of $n \neq k$ in Eq. (1.3) is zero, so there is

$$\begin{aligned} V_{\text{rms}} &= \sqrt{\frac{1}{T}\int_0^T \sum_{n=1}^{\infty} V_n^2 \cos^2 n\omega t \,\mathrm{d}t} \\ &= \sqrt{\frac{1}{T}\int_0^T \sum_{n=1}^{\infty} \frac{V_n^2}{2}(1 + \cos 2n\omega t)\mathrm{d}t} \end{aligned} \tag{1.4}$$

The integral result of the double frequency term in Eq. (1.4) is zero in one complete cycle, so there is

$$V_{\text{rms}} = \sqrt{\sum_{n=1}^{\infty} \frac{V_n^2}{2}}. \tag{1.5}$$

Equation (1.5) could be expressed in terms of the RMS value as follows:

$$V_{\text{rms}} = \sqrt{\sum_{n=1}^{\infty} V_{n,\text{rms}}^2}, \tag{1.6}$$

where $V_{n,\text{rms}}$ is the RMS value of the component at frequency f_n.

The fundamental component in Eq. (1.6) is the desired output and the remaining components can be regarded as "distortion". Considering the fundamental component $V_{1,\text{rms}}$, the above equation turns to be

$$V_{\text{rms}} = V_{1,\text{rms}} \sqrt{1 + \sum_{n=2}^{\infty} \left(\frac{V_{n,\text{rms}}}{V_{1,\text{rms}}}\right)^2} \tag{1.7}$$

The total harmonic distortion (THD) of the voltage is then defined as

$$\text{THD} = \sqrt{\sum_{n=2}^{\infty} \left(\frac{V_{n,\text{rms}}}{V_{1,\text{rms}}}\right)^2}. \tag{1.8}$$

To express the DC voltage utilization of the PWM inverter, it is common to use the ratio of the fundamental amplitude of the output voltage to the DC input voltage V_d of the inverter. For the three-phase SPWM inverter, the maximum output phase voltage is $\frac{V_d}{2}$, so the maximum output line voltage is $\frac{\sqrt{3}}{2}V_d$, that is, the DC voltage utilization is 0.866. For the three-phase inverter with SVPWM control, six voltage space vectors $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$ form a hexagon, as shown in Fig. 1.1. When the resultant voltage vector rotates with an inscribed circle of radius OM, the maximum output phase voltage and line voltage are $\frac{\sqrt{3}}{3}V_d$ and V_d, respectively, and the corresponding DC voltage utilization rate is 1. When the resultant voltage vector rotates with an inscribed circle of radius ON, which represents for the maximum conventional SPWM, the maximum output phase voltage and line voltage are $\frac{V_d}{2}$ and $\frac{\sqrt{3}}{2}V_d$, respectively, which means that the DC voltage utilization rate is 0.866. When the voltage vector operates in the hexagonal shape condition, the maximum output phase voltage and line voltage are $\frac{2}{3}V_d$ and $\frac{2\sqrt{3}}{3}V_d$, then the DC voltage utilization rate is 1.155.

The switching frequency of the PWM method could affect the efficiency and reliability of inverter directly. The higher the switching frequency f_s, the smaller the distortion rate of the AC output current of the inverter, and the smaller the capacity and volume of the filter inductor and capacitor. However, as the switching frequency increases, the switching losses increase, and the performance requirements for the switching device are improved.

The loss generated by the switching process is called the dynamic switching loss, which is related to the switching-on time t_{on} and switching-off time t_{off} of the switch. Assuming that the current flowing through the switching device is I_C when turned on, the voltage across the switching device is V_C when turned off, and the current and voltage rise or fall linearly during the turn-on and turn-off processes, then the current and voltage of the switching device change according to the following rules during the turn-on process.

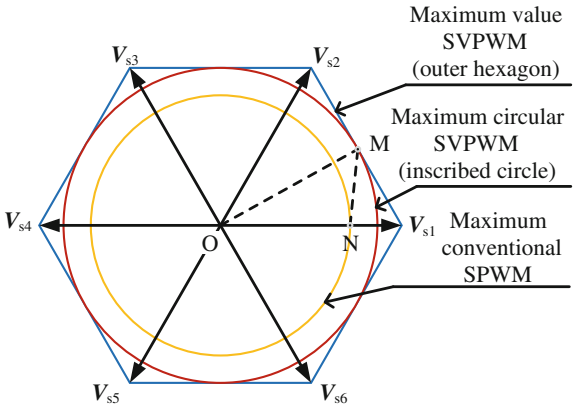


Fig. 1.1 Voltage vectors of a three-phase inverter

$$\begin{cases} i \approx \dfrac{I_C}{t_{on}} t \\ u \approx V_C - \dfrac{V_C}{t_{on}} t \end{cases} \tag{1.9}$$

The expressions of the current and voltage of the switching device during the turn-off process are

$$\begin{cases} i \approx I_C - \dfrac{I_C}{t_{off}} t \\ u \approx \dfrac{V_C}{t_{off}} t \end{cases} \tag{1.10}$$

Then the dynamic switching loss is

$$\begin{aligned} P_S &= f_s \left(\int_0^{t_{on}} \frac{I_C}{t_{on}} t \left(V_C - \frac{V_C}{t_{on}} t \right) \mathrm{d}t + \int_0^{t_{off}} \left(I_C - \frac{I_C}{t_{off}} t \right) \frac{V_C}{t_{off}} t \mathrm{d}t \right) \\ &= \frac{t_{on} + t_{off}}{6} f_s V_C I_C \end{aligned} \tag{1.11}$$

It can be seen that the dynamic switching loss is proportional to the switching frequency f_s. The higher the switching frequency, the larger the loss, the lower the efficiency of the converter, and the switching loss limits the improvement of switching frequency of the converter.

Therefore, various PWM methods for the inverter have been proposed and developed to reduce the harmonic content, increase the DC voltage utilization rate, and reduce the number of switching times. For the AC–AC matrix converter and PWM rectifier, since the former one can be regarded as the AC–DC–AC conversion, the latter one has the same topology as the PWM inverter, their PWM methods can be proposed based on those of inverters.

1.2 SPWM Methods

1.2.1 Natural Sampling SPWM

The natural sampling SPWM method for the inverter is shown in Fig. 1.2 [2], where v_r is a sinusoidal modulating signal and v_c is a triangular carrier signal. The principle of natural sampling SPWM is to compare a sinusoidal modulating voltage of fundamental frequency f_r with a triangular carrier wave of much higher frequency f_c. According to the comparison results, an rectangular pulse sequence whose width

varies with the sinusoidal law is generated, and the pulse sequence is power amplified to drive the inverter to produce a sinusoidal voltage or current output.

Figure 1.3 is a partial enlargement of Fig. 1.2. Accurately calculating the natural intersection time of sine and triangle waveforms is the key to generate a natural SPWM rectangular pulse sequence. Assuming that T_c is the period of the triangular carrier waveform, there are two intersections in one carrier period T_c, which are t_1 and t_2, respectively. Then, the "ON" and "OFF" durations of each SPWM pulse t_{on1}, t_{on2}, t_{off1}, and t_{off2} are determined by

$$\begin{cases} t_{off1} = \dfrac{T_c}{4}(1 - m\sin(\omega t_1)) \\ t_{on1} = \dfrac{T_c}{4}(1 + m\sin(\omega t_1)) \end{cases} \tag{1.12}$$

$$\begin{cases} t_{on2} = \dfrac{T_c}{4}(1 + m\sin(\omega t_2)) \\ t_{off2} = \dfrac{T_c}{4}(1 - m\sin(\omega t_2)) \end{cases} \tag{1.13}$$

where $m = V_{rm}/V_{cm}$ is the modulation ratio; V_{rm} is the peak amplitude of the sinusoidal modulation signal; V_{cm} is the peak amplitude of the triangular signal; m ranges from 0 to 1 and the larger the value it is, the higher the fundamental voltage of the output. ω is the angular frequency of the sine wave, which is the desired fundamental frequency of the inverter output voltage.

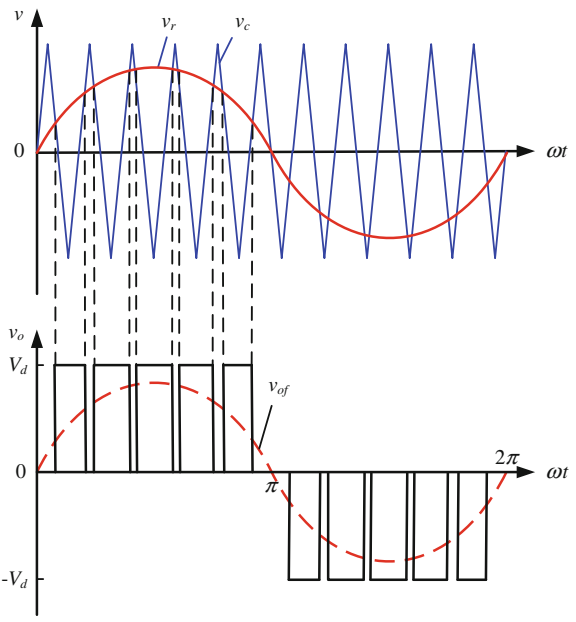


Fig. 1.2 Principle of the SPWM waveform generation

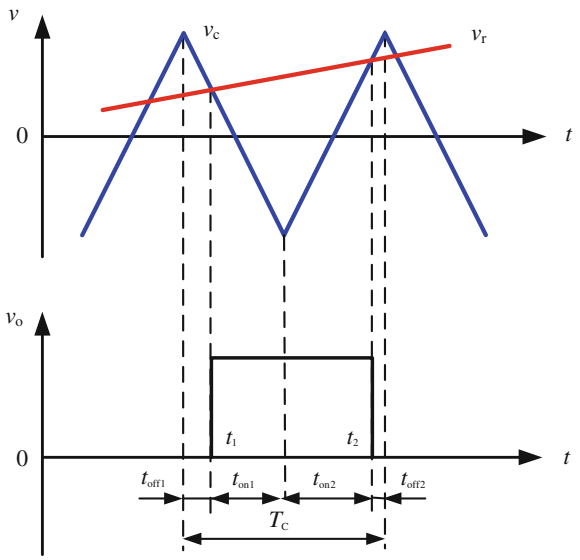


Fig. 1.3 Natural sampling SPWM method

The pulse width of the generated SPWM wave in one period is

$$t_{on} = t_{on1} + t_{on2} = \frac{T_c}{2}\left(1 + \frac{m}{2}(\sin \omega t_1 + \sin \omega t_2)\right) \tag{1.14}$$

Since Eq. (1.14) is a transcendental equation, it will take a lot of time to solve it by the conventional numerical solution. Therefore, it has been considered that the mathematical model of the natural sampling method is not suitable for real-time control.

1.2.2 Symmetric Regular Sampling SPWM

The symmetric regular sampling SPWM method takes the time corresponding to the symmetry axis of each triangular wave as the sampling time. When a vertex is used as the sampling point, the generated pulse width is significantly smaller and the control error is larger, so the bottom point is usually used as the axis of symmetry [3].

As shown in Fig. 1.4, a line passing through the intersection point of the sine wave and the symmetry axis of the triangle wave is parallel to the time axis. The intersection of the parallel line and the triangular wave is sampled as the "ON" or "OFF" moment of the SPWM wave. Since these two intersections are symmetrical, the sampling method is called the symmetric regular sampling method.

From Fig. 1.4, the relationship can be obtained as follows

$$\frac{T_c}{\delta} = \frac{2}{1 + m\sin(\omega t_D)} \tag{1.15}$$

where $\frac{\delta}{2} = t_{on1} = t_{on2}$. Thus, the pulse width can be defined by

$$\delta = \frac{T_c}{2}\left(1 + m\sin\left((2n-1)\frac{\pi}{N}\right)\right) \tag{1.16}$$

where $n = 1, 2, \ldots, N$, $N = \frac{f_c}{f_r}$ is the frequency modulation ratio.

During one period of the triangular wave, the gap width on both sides of the pulse is

$$\delta' = \frac{1}{2}(T_c - \delta) = \frac{T_c}{4}\left(1 - m\sin\left((2n-1)\frac{2\pi}{N}\right)\right) \tag{1.17}$$

For the three-phase half-bridge inverter, a three-phase SPWM wave should be formed. Usually, the triangular carriers are common to the three phases, and the three-phase sinusoidal modulated waves are sequentially $\frac{2\pi}{3}$ out of phase. The pulse widths of the three phases in the same triangular wave period are δ_a, δ_b and δ_c, respectively, and the gap widths are δ'_a, δ'_b and δ'_c, respectively. Since the sum of the three-phase sinusoidal modulating voltages is zero at any time, the following equation is established.

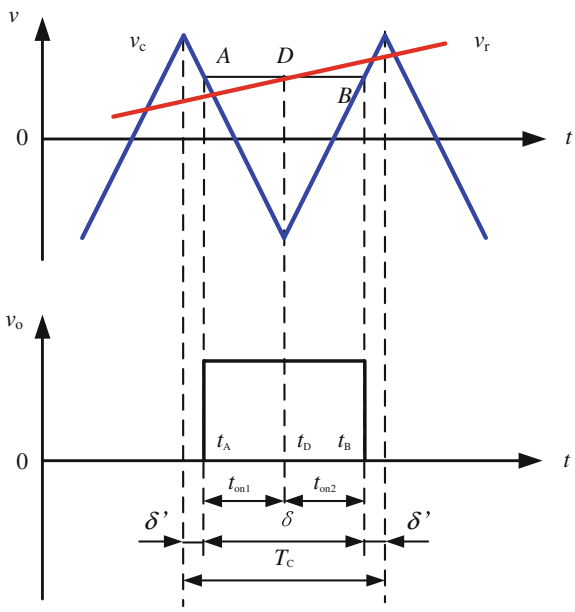


Fig. 1.4 Symmetric regular sampling SPWM

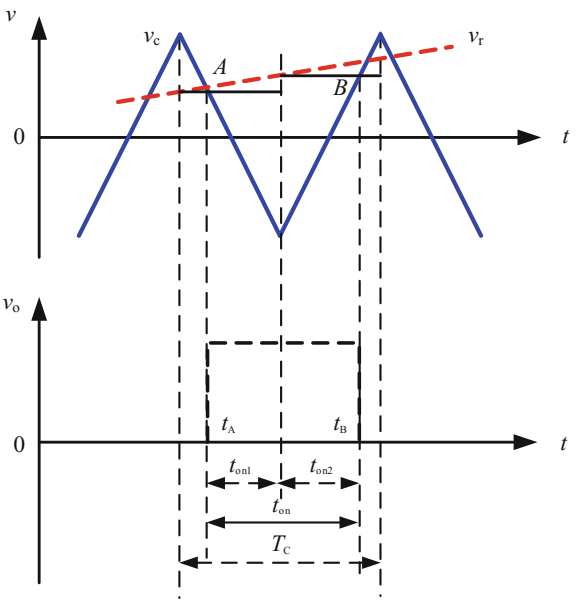


Fig. 1.5 Asymmetric regular sampling SPWM

$$\begin{cases} \delta_a + \delta_b + \delta_c = \dfrac{3}{2} T_c \\ \delta'_a + \delta'_b + \delta'_c = \dfrac{3}{4} T_c \end{cases} \tag{1.18}$$

Generally, both δ_a and δ'_a for phase A can be calculated by the microprocessor first, then δ_b and δ'_b for phase B, δ_c and δ'_c for phase C could be generated by the phase-shifted method.

1.2.3 Asymmetric Regular Sampling SPWM

The mathematical model of the symmetric regular sampling method is very simple, but it is only sampled once per carrier cycle, which results in a large deviation between the formed step wave and the sine wave. If it is sampled at both the peak and bottom positions of the triangle wave, that is, it is sampled twice per carrier cycle, then the formed step wave will be much similar to the sine wave. The principle of the asymmetric regular sampling method is shown in Fig. 1.5 [4].

From Fig. 1.5, the "ON" durations are defined by

$$t_{on1} = \frac{T_c}{4}\left(1 + m \sin \frac{n\pi}{N}\right), \quad n = 0, 2, 4, \ \ldots, \ 2(N-1) \tag{1.19}$$

$$t_{\text{on2}} = \frac{T_{\text{c}}}{4}\left(1 + m\sin\frac{n\pi}{N}\right), \quad n = 1, 3, 5, \ \ldots, \ 2N - 1 \tag{1.20}$$

Obviously, when n is an even number, it represents for the vertex sampling, and when n is an odd number, it represents for the bottom point sampling.

Therefore, the pulse width of the single-phase SPWM wave can be calculated as follows:

$$t_{\text{on}} = t_{\text{on1}} + t_{\text{on2}} \tag{1.21}$$

To generate a three-phase SPWM wave, three sine waves with a phase shift of $\frac{2\pi}{3}$ are compared with one common triangular wave. When the vertexes are sampled, there are

$$\begin{cases} t_{\text{on1}}^{\text{C}} = \dfrac{T_{\text{c}}}{4}\left(1 + m\sin\left(n\dfrac{\pi}{N}\right)\right) \\ t_{\text{on1}}^{\text{B}} = \dfrac{T_{\text{c}}}{4}\left(1 + m\sin\left(n\dfrac{\pi}{N} + \dfrac{2\pi}{3}\right)\right), \quad n = 0, 2, 4, \ \ldots, \ 2(N-1) \\ t_{\text{on1}}^{\text{A}} = \dfrac{T_{\text{c}}}{4}\left(1 + m\sin\left(n\dfrac{\pi}{N} + \dfrac{4\pi}{3}\right)\right) \end{cases} \tag{1.22}$$

When the bottom points are sampled, there are

$$\begin{cases} t_{\text{on2}}^{\text{C}} = \dfrac{T_{\text{c}}}{4}\left(1 + m\sin\left(n\dfrac{\pi}{N}\right)\right) \\ t_{\text{on2}}^{\text{B}} = \dfrac{T_{\text{c}}}{4}\left(1 + m\sin\left(n\dfrac{\pi}{N} + \dfrac{2\pi}{3}\right)\right), \quad n = 1, 3, 5, \ \ldots, \ 2N - 1 \\ t_{\text{on2}}^{\text{A}} = \dfrac{T_{\text{c}}}{4}\left(1 + m\sin\left(n\dfrac{\pi}{N} + \dfrac{4\pi}{3}\right)\right) \end{cases} \tag{1.23}$$

Therefore, the pulse width of each phase of the three-phase SPWM wave can be expressed as follows:

$$\begin{cases} t_{\text{on}}^{\text{C}} = t_{\text{on1}}^{\text{C}} + t_{\text{on2}}^{\text{C}} \\ t_{\text{on}}^{\text{B}} = t_{\text{on1}}^{\text{B}} + t_{\text{on2}}^{\text{B}} \\ t_{\text{on}}^{\text{A}} = t_{\text{on1}}^{\text{A}} + t_{\text{on2}}^{\text{A}} \end{cases} \tag{1.24}$$

In order to make the three-phase SPWM wave symmetrical, the frequency modulation ratio N is preferably selected to be an integral multiple of three.

1.2.4 Equal-Area Sampling SPWM

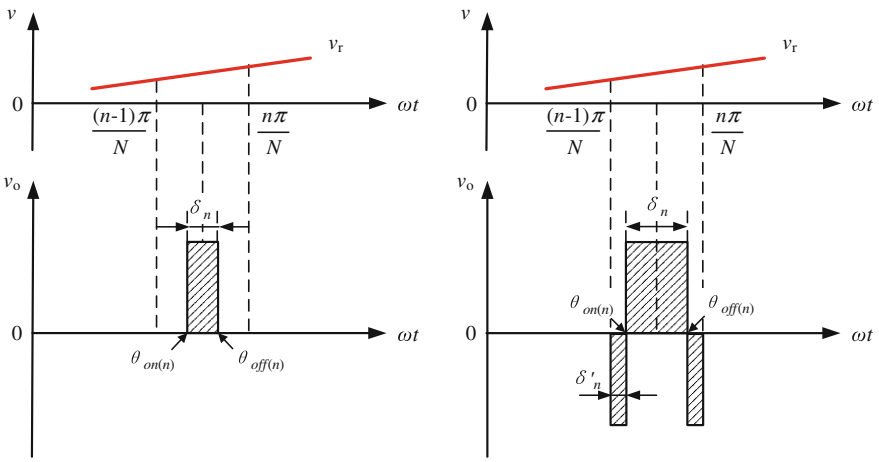
By dividing a sinusoidal half-wave into N equal parts, a series of contoured rectangular pulse with an equal area is used to replace the area surrounded by the sinusoidal wave and the horizontal axis. The midpoint of the rectangular pulse and that of the sine wave coincide, so that the waveform composed of N equal-height unequal-width rectangular pulses is equivalent to the sinusoidal half-wave. Obviously, the width or switching moment of this series of pulse waveforms can be calculated mathematically.

Figure 1.6a shows the schematic diagram of the unipolar equal-area sampling algorithm [5]. When the positive half-cycle of the sinusoidal signal is divided into N equal parts, the width of each part is $\frac{\pi}{N}$. Assuming that the pulse height is $\frac{V_s}{2}$, the pulse width of the nth SPWM pulse is δ_n. Since the nth area of the sine wave is equal to the corresponding nth SPWM pulse area, we have

$$\delta_n = \frac{2V_{rm}}{V_s}\left(\cos\left(\frac{n-1}{N}\pi\right) - \cos\left(\frac{n}{N}\pi\right)\right), \quad n = 1, 2, \ldots, N \tag{1.25}$$

Thus, the switching angles of the nth pulse are determined by

$$\begin{cases} \theta_{on(n)} = \dfrac{1}{2}\left(\dfrac{2n-1}{N}\pi - \delta_n\right) \\ \theta_{off(n)} = \dfrac{1}{2}\left(\dfrac{2n-1}{N}\pi + \delta_n\right) \end{cases} \tag{1.26}$$



(a) Unipolar. **(b)** Bipolar.

Fig. 1.6 Equal-area sampling SPWM

The negative half-cycle of the sinusoidal wave can also be equivalent to a series of rectangular pulses in the same way.

When the bipolar equal-area sampling algorithm is used, similar to the unipolar equal-area sampling algorithm, the sinusoidal half-cycle wave is divided into N equal parts, and the area of the nth part is equal to the area sum of rectangular pulses, as shown in Fig. 1.6b.

The width of the positive and negative pulses are determined by

$$\delta_n = \frac{\pi}{2N} + \frac{U_{\text{rm}}}{U_s}\left(\cos\left(\frac{n-1}{N}\pi\right) - \cos\left(\frac{n}{N}\pi\right)\right), \quad n = 1, 2, \ \ldots, \ N \tag{1.27}$$

$$\delta'_n = \frac{\pi}{4N} - \frac{U_{\text{rm}}}{2U_s}\left(\cos\left(\frac{n-1}{N}\pi\right) - \cos\left(\frac{n}{N}\pi\right)\right), \quad n = 1, 2, \ \ldots, \ N \tag{1.28}$$

Then, the switching angles of the nth pulse are determined by

$$\begin{cases} \theta_{\text{on}(n)} = \dfrac{n-1}{N}\pi + \delta'_n \\ \theta_{\text{off}(n)} = \dfrac{n}{N}\pi - \delta'_n \end{cases} \tag{1.29}$$

1.2.5 Selective Harmonic Elimination PWM

Selective harmonic elimination PWM (SHEPWM) method has been received attention since its introduction in 1973 [6]. SHEPWM method, also known as the optimized PWM method, is designed to optimize a specific objective function, such as minimum loss, reduced current ripple, or selectively elimination of certain harmonics. Therefore, it is an effective way to achieve high-quality output to meet some application standards and improve overall operation performance.

The basic idea of SHEPWM method is to obtain the Fourier series expansion on the specific pulse waveforms by Fourier series analysis, and then set certain specific lower harmonics to zero to obtain a nonlinear equation group reflecting the pulse phase angles. Therefore, the switching angles of the pulse are determined by the solution of the equations, and the generated pulses will not contain the specific lower harmonics.

In order to reduce harmonics and facilitate analysis, the SHEPWM waveform is always set to be symmetrical. Let it be the π half-wave odd symmetry, and then make it $\frac{\pi}{2}$ even symmetrical. The common unipolar SHEPWM waveform is shown in Fig. 1.7, where M is the number of switching angles in $\left[0, \frac{\pi}{2}\right]$.

By using the Fourier series to express the SHEPWM waveform of Fig. 1.7, the harmonic expression of the unipolar SHEPWM method is as follows:

$$V_k = \frac{4V_{\mathrm{dc}}}{k\pi}\left[\sum_{j=1}^{M}(-1)^j \cos\left(k\alpha_j\right)\right] \tag{1.30}$$

where V_k is the amplitude of the kth harmonic, $k = 1, 3, 5, \ldots, 2M-1$.

According to Eq. (1.30), it is possible to calculate all switching angles to satisfy with $0 < \alpha_1 < \alpha_2 < \cdots < \alpha_M < \frac{\pi}{2}$, in order to obtain a predetermined fundamental voltage V_1 and make the specific high harmonics equal to zero.

For the three-phase inverter, the phases of the switching angles in Fig. 1.7 only need to be shifted by $\frac{2\pi}{3}$ and $\frac{4\pi}{3}$, respectively, to form the other two phase angles.

Compared with the natural sampling SPWM method, SHEPWM method has the following advantages:

(1) The switching frequency of the power device decreases, and thus the switching loss could be reduced.
(2) When the number of switching times is equal, the quality of the output voltage and current is higher, which reduces the requirements on the input and output filters.
(3) Through overmodulation, the maximum amplitude of the fundamental voltage can reach 1.15 times of the DC side voltage.
(4) Since the low-order harmonics have been eliminated, the current ripple is greatly reduced, and the performance of the inverter is improved.

The biggest obstacle to the application of SHEPWM method is the difficulty in solving the harmonic elimination model. Since the harmonic elimination model is a nonlinear and transcendental equation group, it is usually solved by the Newton iteration method. However, the Newton iteration method has the property of local convergence. It is necessary to find the initial value close to the exact value first, otherwise, the iteration will not converge. Therefore, the Newton iteration method is

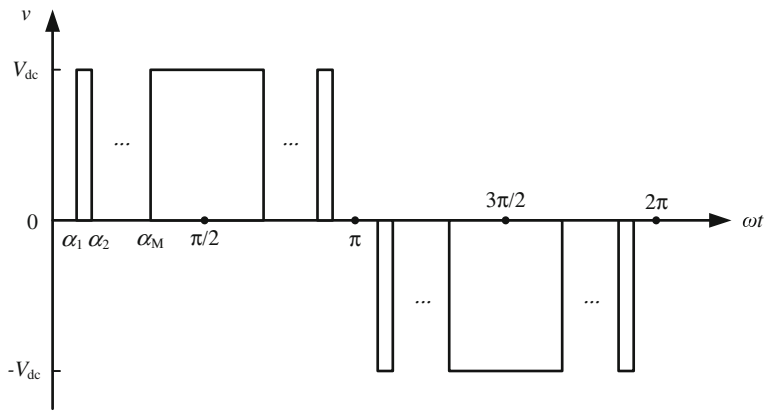


Fig. 1.7 Unipolar SHEPWM

difficult and time-consuming to solve, which is not conducive to online calculation and real-time control.

In addition, SHEPWM method does not eliminate or reduce the total harmonic energy, but only changes the composition of each harmonic. Since the low harmonics are not easy to be eliminated by the filter and have a stronger impact on the electromechanical equipment and external circuits compared with the higher ones, the SHEPWM method only minimizes the low-order harmonics. Therefore, the total harmonic energy is mainly composed of higher harmonics, which are easily filtered.

1.3 SVPWM Method

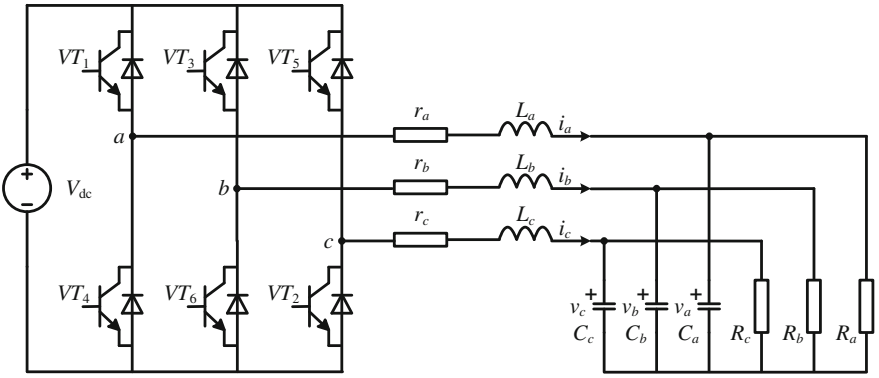
1.3.1 Principle of SVPWM

Space vector PWM (SVPWM) was proposed in the mid-1980s, which aims to produce a circular path of the motor flux linkage, and was first applied to the drive control of asynchronous motors [7]. The principle of SVPWM is shown in Fig. 1.8, in which $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$ and $\vec{V}_{s6}$ are six nonzero basic voltage space vectors of a half-bridge three-phase inverter and constitute six sectors. v_{ref} is the required output reference voltage synthesis space vector, the relationship among the space vectors in a switching cycle is $\int_0^{T_s} \mathrm{v}_{\text{ref}} \mathrm{d}t = \int_0^{T_a} \mathrm{v}_a \mathrm{d}t + \int_0^{T_b} \mathrm{v}_b \mathrm{d}t$, where $v_a, v_b \in \{V_{s1}, V_{s2}, V_{s3}, V_{s4}, V_{s5}, V_{s6}\}$. By using two adjacent voltage space vectors to synthesize the required reference output voltage, the harmonics of the three-phase output line voltage of the inverter v_{ab}, v_{bc} and v_{ca} are the smallest and closer to the sinusoidal waveform, when the resultant voltage space vector trajectory approaches the circle.

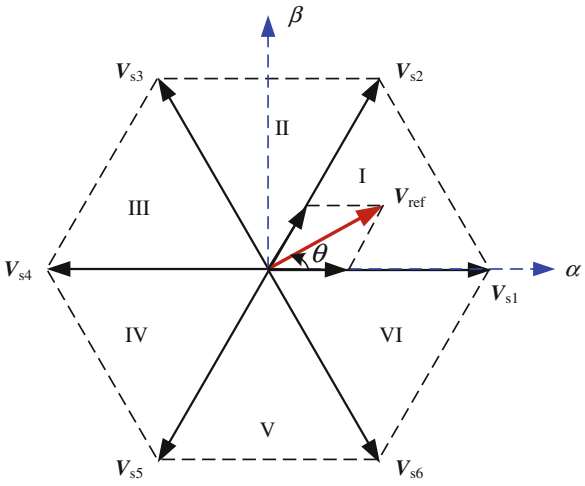
In order to reduce harmonics, the zero voltage space vectors $\vec{V}_{s7}$ and $\vec{V}_{s8}$ are generally inserted uniformly in the SVPWM, but it will increase the number of switching. In addition, since the zero vector duration required at higher frequencies is shorter, the effect of uniformly inserting the zero vectors to reduce the harmonics is not significant, and the harmonics may increase when the dead zone effect is considered.

1.3.2 Relationships Between SPWM and SVPWM

From an implementation point of view, SVPWM and SPWM are very different. SVPWM does not need modulation wave, therefore, it is often regarded as a special PWM. However, both SVPWM and PWM are designed to produce sinusoidal waveforms, there should be an inevitable connection essentially. In fact, SPWM is proposed based on the time-domain area equivalent principle, while SVPWM is



(a) Three-phase voltage-source inverter.



(b) Basic voltage space vectors and sector distribution.

Fig. 1.8 SVPWM principle for the three-phase inverter

based on the equivalent principle of space-rotation voltage vector. For SPWM, the denser the equivalent time-domain area is, the smaller the harmonic is, which is closer to the sinusoidal wave. For SVPWM, there are many ways to synthesize the voltage vectors in each sector, depending on the duration of each elementary voltage vector that constitutes the resultant voltage vector. Thus, the constituent modes of SVPWM are more abundant, SPWM may be one of the SVPWM components. For example, regular sampling SPWM can be considered to be the basic SVPWM with the added zero-space voltage vectors. As another example, by changing the SPWM modulation signal, the output voltage of the SPWM can be the same as that of the SVPWM. Furthermore, SVPWM can be regarded as an SPWM with the smallest

harmonic objective function. However, these studies are based on the equivalent output performance to judge the relationship between SPWM and SVPWM, while there lacks a strict proof mathematically. The relationship between SVPWM and SPWM is still under discussion.

At present, compared with SPWM, SVPWM has the following obvious advantages: (1) The utilization ratio of DC voltage can be increased by 15%; (2) The number of switching can be reduced by 1/3; (3) Better harmonic suppression effect can be achieved; (4) Digital control is easy to be implemented. However, the conventional SVPWM method needs complex trigonometric functions and coordinate rotation operations, and the complex algorithm has a great impact on high precision real-time control.

1.4 Proposition of *m*-Mode SVPWM

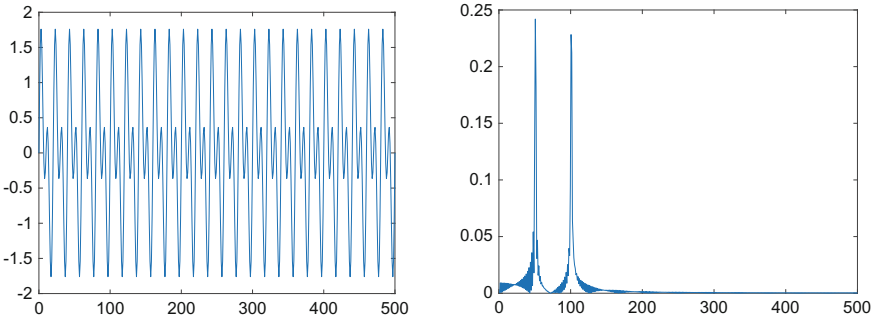
1.4.1 Multi-solution Problem of SPWM

As described in Sect. 1.1, the mathematical basis of SPWM is the Fourier series analysis. However, the Fourier series analysis method has only frequency domain resolution, but no time-domain resolution. Figure 1.9 shows two completely different time-domain signals, but their frequency spectrums are almost the same. That is, the frequency domain expression and time-domain expression of the signal are not one-to-one correspondence, and the same frequency domain expression has multiple solutions in the time domain. Therefore, under the same harmonic requirements, the output voltage of the inverter may have different SPWM waveforms, which makes the SPWM not achieve the intended purpose in practical applications.

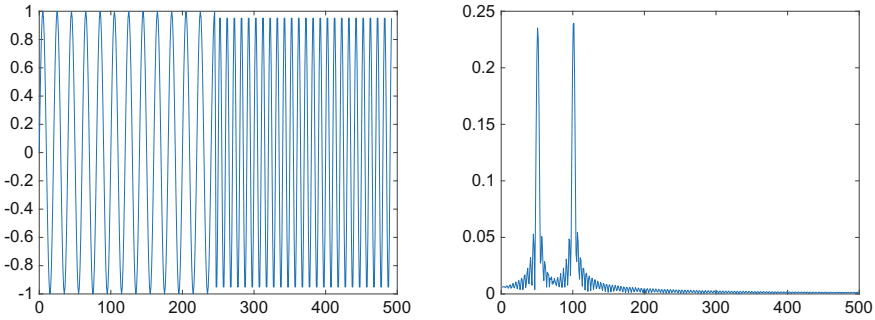
For example, in SHEPWM, when calculating the time-domain switching angle of a waveform according to the Fourier series expansion, there are two solutions for each switching angle. Two kinds of SHEPWM waveforms are shown in Fig. 1.10a and b, respectively. As a result, the inverter could output a waveform with the first set of switching angle solutions in the positive half-cycle, while output a waveform with the second set of switching angle solutions in the negative half-cycle, as shown in Fig. 1.10c, the asymmetry of the waveform will increase the harmonics.

1.4.2 Computing Complex Problem of SVPWM

The biggest difficulty of SVPWM lies in the computational complexity, which is concentrated in the difficulty of judging the sector in which the reference voltage space vector is located, and thus it is difficult to obtain the switching control states of the converter required for the vector synthesis operation. The complexity of computation increases dramatically as the number of output levels increases. For example, for a



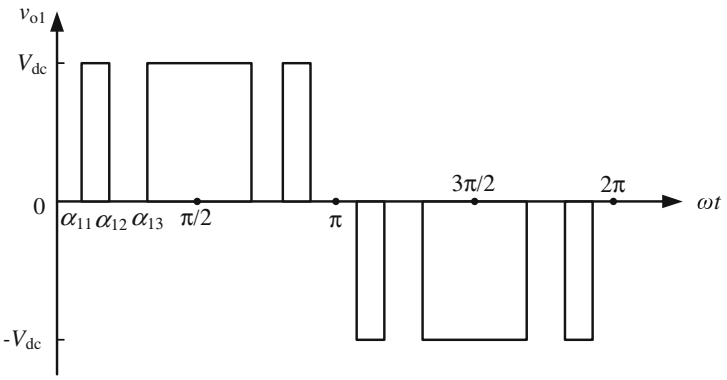
(a) $v = V_{m1}\sin\omega t + V_{m2}\sin 2\omega t$.



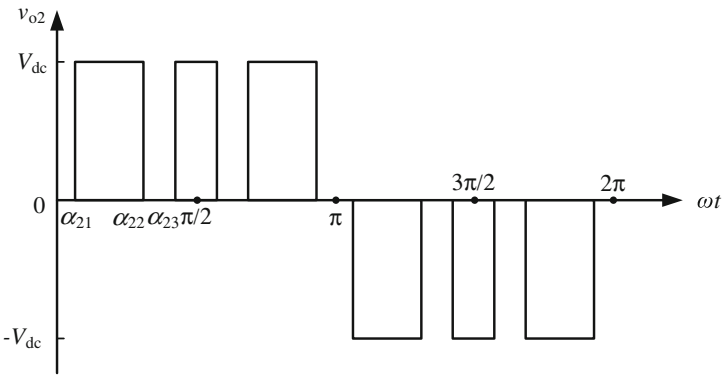
(b) $$v = \begin{cases} V_{m1}\sin\omega t & 0 \le t < \dfrac{T}{2} \\ V_{m2}\sin 2\omega t & \dfrac{T}{2} \le t < T \end{cases}.$$

Fig. 1.9 Spectrum distribution of different signals

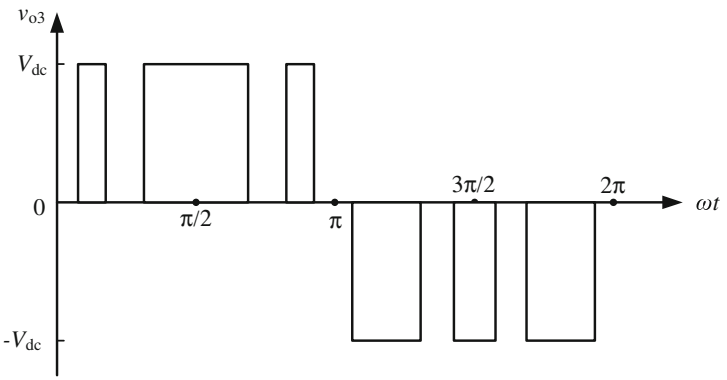
two-level three-phase inverter, there are 8 basic space voltage vectors and 6 sectors; for a three-level three-phase inverter, there are 27 basic space voltage vectors and 24 sectors. In order to determine the sector in which the reference voltage synthesis vector is located, a large number of inverse trigonometric functions, square roots, and trigonometric functions are required. Thus, the accuracy and speed of the calculation are difficult to guarantee, and it must be implemented by hardware circuits. However, when the number of voltage levels is more than 3, it is difficult to perform real-time control of the SVPWM even using a high-performance hardware system. Therefore, simplifying the calculation of SVPWM has become the main research issue at present.



(a) Output voltage with the first set of switching angle solutions.



(b) Output voltage with the second set of switching angle solutions.



(c) Output voltage with both sets of switching angle solutions.

Fig. 1.10 Different SHEPWM waveforms of a single-phase inverter

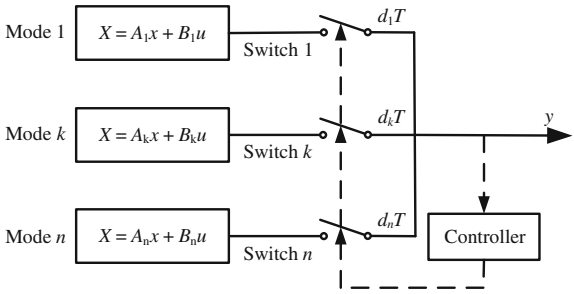


Fig. 1.11 Description of the switched linear system

1.4.3 Ideal of m*-Mode SVPWM*

In view of the fact that there is no one-to-one correspondence between time domain and frequency domain of the SPWM signal, wavelet modulation (WM) method based on wavelet analysis theory [8–10] was proposed in 2007 and has applied to different kinds of inverters. Since wavelet analysis is a localized time–frequency analysis method, it solves the key problem of time-frequency unification compared with the Fourier analysis of the overall signal. In addition, WM can also minimize the PWM transient harmonics. However, the amount of calculation of WM is larger than that of SVPWM, and it is difficult to realize real-time modulation. Therefore, although the calculation of SVPWM is very complicated, SVPWM is more widely used in inverters and other types of converters because its overall performance is better than SPWM.

In order to solve the computational complexity of SVPWM, many simplified algorithms have been proposed successively. However, these algorithms are only used to improve the calculation of inverse trigonometric functions, square roots, and trigonometric functions, which substantially do not improve computational efficiency and are not general.

Obviously, if the number of basic voltage space vectors or the number of sectors can be reduced, it is possible to solve the computational difficulty of SVPWM, but the premise is that the inverter can still output the required voltage waveform. Since the power electronic converter is a typical switched linear system, the switched linear system theory provides the possibility to simplify the calculation of SVPWM. As shown in Fig. 1.11, each operating mode of the half-bridge three-phase inverter can be regarded as a subsystem which outputs a basic voltage space vector, and n subsystems represent for n basic voltage space vectors. According to the SVPWM switching law, the subsystems are controlled to be switched on or off, and then the converter can output the required voltage or current waveform.

Based on the switched linear system theory [11, 12], not all subsystems need to participate in the operation to achieve the expected control effect, as long as the state controllability conditions are met [13, 14]. That is, only m ($m \leq n$) operating modes are needed. In other words, the SVPWM of power electronic converter can be implemented with only a minimum of m basic voltage space vectors. Obviously, when

$m < n$, the voltage space vector of SVPWM has been reduced, as well as the number of sectors, so that the amount of calculation of SVPWM has been reduced. The reduction in the number of sectors reduces the switching number of operation modes or subsystems, which in turn reduces the number of switching and the switching loss, and improves the efficiency of the power electronic converter. Therefore, this monograph proposes the m-mode SVPWM based on the controllability theory of switched linear systems.

1.5 Arrangement of This Book

According to the theory of switched linear systems, this monograph puts forward the state controllability criterion of power electronic converters. The state controllability analysis of two-level three-phase inverter, nine-switch three-phase dual-output inverter, five-phase three-phase dual-output inverter, three-level three-phase inverter, modular multilevel three-phase inverter, and the PWM rectifier will be carried out, the corresponding m-mode SVPWM method will be proposed and verified by the simulation and experimental results. The book is divided into nine chapters, the content is arranged as follows.

This chapter introduces the basic content of PWM, explains the basic principle of SPWM and SVPWM, and proposes the basic idea of m-mode SVPWM based on the discussion of the existed problems of SPWM and SVPWM.

Chapter 2 introduces the basic concept of the switched linear system, focuses on the state controllability theory of switched linear system, and then proposes the m-mode state controllability criterion and the m-mode SVPWM mechanism.

Chapter 3 establishes the switched linear system model of the three-phase four-wire inverter based on its operating principle first. Then the m-mode controllability of for the three-phase four-wire inverter has been analyzed, and it is proven theoretically that the three-phase four-wire inverter has the controllability of 3-mode. Finally, the 3-mode SVPWM for the three-phase four-wire inverter is proposed and verified, which can be extended to the three-phase three-wire inverter.

In Chap. 4, the three-phase four-wire inverter is also theoretically proven to have the controllability of 4-mode, and the corresponding 4-mode SVPWM is proposed. In addition, the similarities and differences between the 4-mode SVPWM and the 3-mode SVPWM are compared, then the geometric meaning of the m-mode SVPWM is revealed. Finally, the construction method of other kinds of m-mode SVPWM has been summarized for the three-phase four-wire inverter.

Chapters 5 and 6 study the dual-output nine-switch inverter and the dual-output five-leg inverter, respectively. By establishing their switched linear system models, the m-mode controllability of the dual-output nine-switch inverter and the dual-output five-leg inverter have been analyzed, and it is proven that both inverters have 6-mode controllability in theory. Then, the 6-mode SVPWMs for the nine-switch inverter and the five-leg inverter are proposed and verified by experimental results.

Chapter 7 applies the *m*-mode SVPWM to multilevel inverters and takes the diode-clamped three-level inverter as an example. It is proven that the three-level inverter is 6-mode controllable. Then, different kinds of *m*-mode SVPWM, such as 6-mode, 9-mode, 12-mode, and 18-mode SVPWMs, are proposed for the three-level inverter. By comparing the 18-mode SVPWM with the traditional SVPWM, the switching sequence of 18-mode SVPWM is simpler than that of traditional SVPWM, which reduces the calculation amount of modulation algorithm and improves the efficiency effectively.

The modular multilevel converter (MMC) is suitable for high-voltage applications, but as the voltage level and the number of sub-modules increases, the SVPWM control for MMC becomes complicated. In Chap. 8, a design method to simplify the topology of MMC sub-module is proposed based on the principle of *m*-mode state controllability. By reducing the number of switching devices in the sub-module, the PWM strategy of MMC can be simplified, which provides a novel application of the *m*-mode state controllability in power converters.

In Chap. 9, the *m*-mode SVPWM method is applied to the voltage-source PWM rectifier. By establishing the switched linear system model of the three-phase PWM rectifier, it is theoretically proven that the three-phase PWM rectifier has the same 3-mode controllability as the three-phase four-wire inverter. Then, 3-mode and 4-mode SVPWMs are proposed for the three-phase PWM rectifier and verified by simulations.

References

1. Holmes DG, Lipo TA (2003) Pulse width modulation for power converters: principle and practice. Wiley Ltd., Chichester
2. Hamman J, Van Der Merwe FS (1988) Voltage harmonics generated by voltage-fed inverters using PWM natural sampling. IEEE Trans Power Electron 3(3):297–302
3. Bowes SR (1990) Regular-sampled harmonics elimination/minimization PWM techniques. In: The 5th annual proceedings on applied power electronics conference and exposition, Los Angeles, CA, USA, 11–16 Mar
4. Bowes SR, Clark PR (1992) Simple microprocessor implementation of new regular-sampled harmonic elimination PWM techniques. IEEE Trans Ind Appl 28(1):89–95
5. Chin TH, Nakano M, Fuwa Y (1984) New PWM technique using a triangular carrier wave of saturable amplitude. IEEE Trans Ind Appl IA-20(3):643–650
6. Patel HS, Hoft RG (1973) Generalized techniques of harmonic elimination and voltage control in thyristor inverters: part I—harmonic elimination. IEEE Trans Ind Appl IA-9(3):310–317
7. Van Der Broeck HW, Skudelny HC, Stanke GV (1988) Analysis and realization of a pulsewidth modulator based on voltage space vectors. IEEE Trans Ind Appl 24(1):142–150
8. Saleh SA, Moloney CR, Rahman MA (2009) Development and testing of wavelet modulation for single-phase inverters. IEEE Trans Ind Electron 56(7):2588–2599
9. Saleh SA, Moloney CR, Rahman MA (2011) Analysis and development of wavelet modulation for three-phase voltage-source inverters. IEEE Trans Ind Electron 58(8):3330–3348
10. Zheng CF, Zhang B, Qiu DY et al (2015) Wavelet PWM technique for single-phase three-level inverters. J Power Electron 15(6):1517–1523
11. Schaft AVD, Schumacher H (2000) An introduction to hybrid dynamical systems. Springer, Berlin

12. Sun ZD, Ge SS (2005) Switched linear systems: control and design. Springer, Berlin
13. Xie GM, Zheng DZ, Wang L (2002) Controllability of switched linear systems. IEEE Trans Autom Control 47(8):1401–1405
14. Sun ZD, Ge SS, Lee TH (2002) Controllability and reach ability criteria for switched linear systems. Automatica 38:775–786

Chapter 2
m-Mode SVPWM Principle of Power Electronic Converter

The power electronic converter achieves the required output performance by turning on or off the power switching components, and its operating mode can be modeled by the piecewise differential equation. Since the model of power electronic converter is consistent with that of the switched linear system, this chapter directly introduces the concept and definition of the state controllability of power electronic converter, derives the criterion of state controllability, and proposes the principle of *m*-mode SVPWM.

2.1 Definition of State Controllability

For a power electronic converter with n different operating modes, the general form of its switched linear system model can be expressed as follows [1–4]:

$$\begin{cases} \dot{x}(t) = A_\sigma x(t) + B_\sigma u(t) \\ y(t) = C_\sigma x(t) \end{cases} \tag{2.1}$$

where $x(t) \in R^p$ is the continuous state variable of the converter, $y(t) \in R^q$ is the output state variable of the converter, $u(t) \in \mathbf{R}^r$ is the system input, and $A_\sigma \in \mathbf{R}^{p\times p}$, $B_\sigma \in \mathbf{R}^{p\times 1}$, and $C_\sigma \in \mathbf{R}^{1\times q}$ are the coefficient matrixes of the state equation. $\sigma \in (1, 2, \ldots, i, \ldots, n)$ is the control variable of the system, which is used to indicate the current operating mode. Only one operating mode is active at any time, that is, if $\sigma = i$, then the converter is operating at the ith mode. Thus, σ can be described by the following switching sequence:

$$\sigma(t) = \psi\left(x(t), y(t), z(t), \sigma^-\right) \tag{2.2}$$

where σ^- is the operating mode at the last moment, $z(t)$ is the external signal of the converter, such as the carrier signal, the given reference signal, etc. Equation (2.2)

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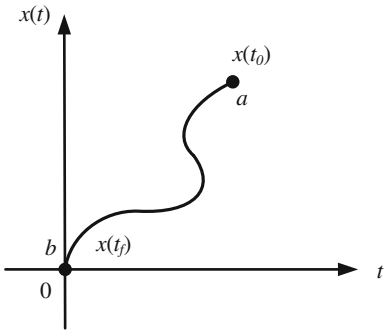

Fig. 2.1 Diagram of state controllability

can also be referred to as the control strategy or switching sequence of the converter. According to the current state variables, the output variables and the parameters of the converter model, the switching control signal can be generated by a specific algorithm to control each operating mode of the converter to work alternately. Obviously, Eqs. (2.1) and (2.2) can clearly reflect the operating law of the converter, that is, according to the initial state of the system, the current operating mode σ is determined by Eq. (2.2), then the state variable $x(t)$ and output variable $y(t)$ can be calculated by Eq. (2.1), and then the operating mode of the next moment is determined according to Eq. (2.2). In this way, the power electronic converter can be switched and controlled according to the control requirements to obtain the required voltage and current output.

For the switched linear system in Eq. (2.1), if the state variables $x(t)$ and $y(t)$ can be controlled by the input $u(t)$ and the switching sequence σ, then this system is considered to be state controllable. Therefore, the state controllability can be defined based on the switched linear system model of the converter,

Definition 2.1 (*State controllability of the converter*) [2, 3, 5] For a switched linear system model as shown in Eq. (2.1), given a nonzero initial state x_0, if there is an input $u(t)$ and a switching sequence σ, the system state can be transferred from $x(t_0) = x_0$ to $x(t_\mathrm{f}) = 0$ in a finite time $t \in [t_0, t_\mathrm{f}]$, then system state x_0 is said to be controllable at time t_0.

The state controllability of the switched linear system can be divided into incomplete controllability and complete controllability, which can be explained by Fig. 2.1. For a point a on the state plane, if there is a specific input $u(t)$ and a corresponding switching sequence σ which can transfer the system state from point a to point b (or the coordinate origin), then this state is said to be incompletely controllable. If there is a corresponding switching sequence regardless of the position of point a in the state plane, point a can be transferred to the coordinate origin, then the system is considered to be completely controllable. Thus, the complete controllability of the system state means that the trajectory of system state variable can cover the whole state plane, that is, the whole plane $(t, x(t))$ shown in Fig. 2.1.

2.2 Criterion of State Controllability

The existing converter analysis method is used to study whether the converter switched linear system model is incompletely controllable or completely controllable, which can be expressed by the following iterative equations according to Eq. (2.1).

$$\begin{aligned} x(t) = {} & e^{A_k h_k} e^{A_{k-1} h_{k-1}} \cdots e^{A_i h_i} \cdots e^{A_1 h_1} x_0 \\ & + e^{A_k h_k} e^{A_{k-1} h_{k-1}} \cdots e^{A_i h_i} \cdots e^{A_2 h_2} \int_0^{h_1} e^{A_1 (h_1 - t)} B_1 u(t) \mathrm{d}t \\ & + \cdots + e^{A_k h_k} \int_{h_1+h_2+\cdots+h_{k-2}}^{h_1+h_2+\cdots+h_{k-1}} e^{A_{k-1}(h_1+h_2+\cdots+h_{k-1}-t)} B_{k-1} u(t) \mathrm{d}t \\ & + \int_{h_1+h_2+\cdots+h_{k-1}}^{h_1+h_2+\cdots+h_k} e^{A_k (h_1+h_2+\cdots+h_k-t)} B_k u(t) \mathrm{d}t \end{aligned} \tag{2.3}$$

where h_i is the duration of the corresponding operating mode of the converter when $\sigma = i$. According to Definition 2.1, if Eq. (2.3) is controllable, then there is $x(t_\mathrm{f}) = 0$ at $t = t_\mathrm{f} = \sum_{i=1}^{k} h_i$.

However, in general, the duration h_i of the operating mode is a function of system state variables, output variables, and control strategy, which is difficult to be determined. Therefore, it is impossible to judge the controllability of the converter by the direct calculation of Eq. (2.3). In particular, when it is required to verify whether the converter is completely state controllable, it is necessary to calculate the controllability of all states on the whole state plane. Obviously, it is impractical to calculate and analyze the controllability of the converter at each state point, so it is necessary to establish the controllability criterion of the converter according to the theory of the switched linear system.

Criterion 2.1 (Controllability criterion of the converter) [2, 6] For the converter shown in Eq. (2.1), the following linear subspace sequences are defined:

$$W_1 = \sum_{\sigma=1}^{n} \langle A_\sigma | B_\sigma \rangle, \; W_2 = \sum_{\sigma=1}^{n} \langle A_\sigma | W_1 \rangle, \; \ldots, \; W_n = \sum_{\sigma=1}^{n} \langle A_\sigma | W_{n-1} \rangle \tag{2.4}$$

where $\langle A_\sigma | B_\sigma \rangle = \sum_{i=1}^{n} A_\sigma^{i-1} B_\sigma$, $\langle A_\sigma | W_1 \rangle = \sum_{i=1}^{n} A_\sigma^{i-1} W_1$, $\ldots$, $\langle A_\sigma | W_{n-1} \rangle = \sum_{i=1}^{n} A_\sigma^{i-1} W_{n-1}$

According to the definition of state controllability, if the system state shown in Eq. (2.1) is completely controllable, then the rank of the matrix W_n is equal to the number of converter state variables p, that is,

$$\text{rank}[W_n] = p \tag{2.5}$$

Equation (2.5) shows that it is possible to determine whether the converter is state controllable by the coefficient matrix of the switched linear system model of Eq. (2.1) without calculating Eq. (2.3).

However, Eqs. (2.4) and (2.5) have a large amount of calculation and are only used when the number of operating modes of the converter is small. According to the switched linear system theory [1], calculating Eq. (2.5) is equivalent to calculating the rank of the following matrix:

$$\begin{aligned}\text{rank}[&B_1,\ \ldots,\ B_n, A_1B_1,\ \ldots,\ A_nB_1,\ \ldots,\ A_1B_n,\ \ldots,\ A_nB_n,\\ &A_1^2B_1,\ \ldots,\ A_nA_1B_1,\ \ldots,\ A_1^2B_n,\ \ldots,\ A_nA_1B_n,\ \ldots,\\ &A_1^{n-1}B_1,\ \ldots,\ A_nA_1^{n-2}B_1,\ \ldots,\ A_1A_n^{n-2}B_n,\ \ldots,\ A_n^{n-1}B_n\Big] = p\end{aligned} \tag{2.6}$$

Equation (2.6) is a matrix of $p \times p_n$ dimensions, where $p_n = \frac{n(1-n^n)}{1-n}$. For the convenience of calculation, Eq. (2.6) can be rewritten as

$$\text{rank}\left[\widehat{B},\ \widehat{A}_1,\ \widehat{A}_2,\ \ldots,\ \widehat{A}_{n-1}\right] = p \tag{2.7}$$

where $\widehat{B} = [B_1, B_2, \ldots, B_n]$ is a $p \times n$-dimensional matrix, $\widehat{A}_1 = \left[A_1\widehat{B}, A_2\widehat{B}, \ldots, A_n\widehat{B}\right]$ is a $p \times n^2$-dimensional matrix, $\widehat{A}_2 = \left[A_1\widehat{A}_1, A_2\widehat{A}_1, \ldots, A_n\widehat{A}_1\right]$ is a $p \times n^3$-dimensional matrix, $\widehat{A}_3 = \left[A_1\widehat{A}_2, A_2\widehat{A}_2, \ldots, A_n\widehat{A}_2\right]$ is a $p \times n^4$-dimensional matrix, …, and $\widehat{A}_{n-1} = \left[A_1\widehat{A}_{n-2}, A_2\widehat{A}_{n-2}, \ldots, A_n\widehat{A}_{n-2}\right]$ is a $p \times n^n$-dimensional matrix.

Therefore, the ranks of $\widehat{B}, \widehat{A}_1, \widehat{A}_2, \widehat{A}_3, \ldots, \widehat{A}_{n-1}$ can be calculated successively. Once the above calculation result is equal to the number of converter state variables p, it can be known that the converter is state controllable, there is no need to calculate the rank of Eq. (2.7).

2.3 m-Mode Controllability

Based on the system control principle, for any control system, if there are p state variables, only p control inputs are needed to achieve state control in theory. For a converter with control variable $\sigma \in (1, 2, \ \ldots, \ i, \ \ldots, \ n)$, that is, n operating modes among σ can be used as a control variable alone, a combination of multiple operating modes can be used as a control variable as well. Obviously, the number of possible control variables is greater than p, that is, the number of control variables is greater than the number of state variables, and there is redundancy. Therefore, selecting m ($m \leq n$) operating modes from σ, if the number of combined variables of m operating modes is equal to the number of converter state variables p, then the converter control conditions will be satisfied without all operating modes to participate in the operation. Since m operating modes correspond to $\sum_{i=1}^{m} \binom{m}{i}$ control variables, if the following equation is established:

$$\sum_{i=1}^{m} \binom{m}{i} \geq p \tag{2.8}$$

then the m operating modes may achieve state controllability of the converter. According to Eq. (2.8), the definition and criterion of m-mode controllability of the converter are proposed.

Definition 2.2 (*m-mode controllability of the converter*) [3] For a converter shown in Eq. (2.1), which has p state variables and n operating modes, given a nonzero initial state x_0, the converter state x_0 is said to be m-mode controllable at time t_0, if there is an input $u(t)$ and a control variable combined by m ($m \leq n$) operating modes, such that the converter can be transferred from $x(t_0) = x_0$ to $x(t_\mathrm{f}) = 0$ within a finite time $t \in [t_0, t_\mathrm{f}]$.

Criterion 2.2 (m-mode controllability criterion of the converter) [3, 6] For a converter shown in Eq. (2.1), the following linear subspace sequences are defined:

$$W_1' = \sum_{\sigma'=1}^{m} \langle A_{\sigma'} | B_{\sigma'} \rangle, \quad W_2' = \sum_{\sigma'=1}^{m} \left\langle A_{\sigma'} \middle| W_1' \right\rangle, \ \ldots, \ W_m' = \sum_{\sigma'=1}^{m} \left\langle A_{\sigma'} W_{m-1}' \right\rangle \tag{2.9}$$

where $\langle A_{\sigma'} | B_{\sigma'} \rangle = \sum_{i=1}^{m} A_{\sigma'}^{i-1} B_{\sigma'}$, $\left\langle A_{\sigma'} \middle| W_1' \right\rangle = \sum_{i=1}^{m} A_{\sigma'}^{i-1} W_1'$, $\ldots$, $\left\langle A_{\sigma'} \middle| W_{m-1}' \right\rangle = \sum_{i=1}^{m} A_{\sigma'}^{i-1} W_{m-1}'$. $A_{\sigma'}$ and $B_{\sigma'}$ are the coefficient matrices of the m operating modes of the original A_σ and B_σ, and are reordered under the switching operation sequence $\sigma' \in (1, 2, \ \ldots, \ m)$.

If the rank of the matrix W_m' is equal to the number of the converter state variables p, that is

$$\operatorname{rank}\left[W'_m\right] = p \tag{2.10}$$

Then the converter shown in Eq. (2.1) is m-mode controllable.

The definition of Eq. (2.9) and the criterion of Eq. (2.10) determine the basic characteristic of m-mode controllability. The m-mode controllability actually proves that the converter has the controllable characteristic with the least operating modes. It also shows that the state controllability of the converter can be realized by a combination of different operating modes, as a result, there will be multiple types of m-mode controllability.

Similar to Eq. (2.6), the rank of the matrix W'_m can be equivalently calculated by

$$\begin{aligned}\operatorname{rank}\big[&B'_1,\ \ldots,\ B'_m, A'_1B'_1,\ \ldots,\ A'_mB'_1,\ \ldots,\ A'_1B'_m,\ \ldots,\ A'_mB'_m,\\ &A_1^{'2}B'_1,\ \ldots,\ A'_mA'_1B'_1,\ \ldots,\ A_1^{'2}B_m,\ \ldots,\ A'_mA'_1B'_m,\ \ldots,\\ &A_1^{'m-1}B'_1,\ \ldots,\ A'_mA_1^{'m-2}B'_1,\ \ldots,\ A'_1A_1^{'m-2}B'_m,\ \ldots,\ A_m^{'m-1}B'_m\big] = p\end{aligned} \tag{2.11}$$

Equation (2.11) is a $p \times p_m$-dimensional matrix, where $p_m = \frac{m(1-m^m)}{1-m}$. Equation (2.11) is rewritten as

$$\operatorname{rank}\left[\widehat{B}^{'}, \widehat{A}_1^{'}, \widehat{A}_2^{'},\ \ldots,\ \widehat{A}_{m-1}^{'}\right] = p \tag{2.12}$$

where $\widehat{B}^{'} = \left[B'_1, B'_2,\ \ldots,\ B'_m\right]$ is a $p \times m$-dimensional matrix, $\widehat{A}_1^{'} = \left[A'_1\widehat{B}^{'}, A'_2\widehat{B}^{'},\ \ldots,\ A'_m\widehat{B}^{'}\right]$ is a $p \times m^2$-dimensional matrix, $\widehat{A}_2^{'} = \left[A'_1\widehat{A}_1^{'}, A'_2\widehat{A}_1^{'},\ \ldots,\ A'_m\widehat{A}_1^{'}\right]$ is a $p \times m^3$-dimensional matrix, $\widehat{A}_3^{'} = \left[A'_1\widehat{A}_2^{'}, A'_2\widehat{A}_2^{'},\ \ldots,\ A'_m\widehat{A}_2^{'}\right]$ is a $p \times m^4$-dimensional matrix, $\cdots$, and $\widehat{A}_{m-1}^{'} = \left[A'_1\widehat{A}_{m-2}^{'}, A'_2\widehat{A}_{m-2}^{'},\ \ldots,\ A'_m\widehat{A}_{m-2}^{'}\right]$ is a $p \times m^m$-dimensional matrix.

Similar to the calculation method of Eq. (2.7), the ranks of $\widehat{B}^{'}, \widehat{A}_1^{'}, \widehat{A}_2^{'}, \widehat{A}_3^{'},\ \ldots,\ \widehat{A}_{m-1}^{'}$ are successively calculated. Once the above calculation result is equal to the number of converter state variables p, it is concluded that the converter is m-mode controllable.

2.4 m-Mode SVPWM

The purpose of SVPWM is to make a three-phase inverter output a three-phase symmetrical sinusoidal voltage. Therefore, according to the principle of SVPWM,

the trajectory of the synthesis voltage space vector formed by the basic voltage space vectors of the three-phase inverter should be circular. Since the existed voltage space vectors of three-phase inverter are all synthesized by using all basic voltage vectors, that is, all the operating modes of the three-phase inverter are involved in the operation. Consequently, the more complicated the three-phase inverter topology is, the more the number of output level is, and the number of operating modes, as well as the computational complexity of SVPWM, increases exponentially. The *m*-mode controllability of the converter indicates that the inverter can be state controllable without all operating modes participating in the operation. Therefore, the SVPWM technology of the inverter can be realized based on the *m*-mode controllability.

Theorem 2.1 (*m*-mode SVPWM theorem of three-phase inverter) [3] *For a three-phase inverter with n operating modes, only m* ($m \leq n$) *operating modes are needed to realize inverter state control, then the synthesis voltage space vector can be formed to realize SVPWM by m basic voltage space vectors corresponding to m operating modes.*

The *m*-mode SVPWM theorem of three-phase inverter shows that SVPWM has multiple implementation methods, and there is a minimum operating mode implementation technique, that is, SVPWM can be implemented by a minimum number of basic voltage space vectors. SVPWM has a corresponding relationship with the state controllability of the inverter, the state controllability of the inverter is the basis of SVPWM, which reveals the essence of SVPWM.

Theorem 2.1 is proposed for three-phase inverters, but is also applicable to three-phase AC–DC and AC–AC converters using SVPWM. In addition, the *m*-mode SVPWM of three-phase inverter can realize redundant modulation. If some of the operating modes cannot participate in operation due to the fault, then *m*-mode SVPWM can still be realized by using other available operating modes, as long as the number of remaining operating modes are still greater than or equal to *m*, and meets with the *m*-mode controllability conditions.

2.5 Summary

Based on the switched linear system model and switched linear system theory, the definition of converter state controllability for power electronic converter has been proposed in this chapter, and the criterion of converter state controllability has been established, which is the system can achieve state controllability only if the number of state variables is equal to the number of control variables. Furthermore, the definition of *m*-mode controllability for the power electronic converter has been proposed and the criterion of *m*-mode controllability has been established, because in the general situation, the number of control variables is greater than that of the state variables and the number of control variables is redundant. Finally, the *m*-mode SVPWM principle of the three-phase inverter has been proposed, which is not only suitable

for the three-phase inverters, but also for three-phase AC–DC and AC–AC converters using SVPWM.

References

1. Sun ZD, Ge SZ (2005) Switched linear systems: control and design. Springer, Germany
2. Xie G, Zheng DZ, Wang L (2002) Controllability of switched linear systems. IEEE Trans Autom Control 47(8):1401–1405
3. Li XF, Zhang B, Qiu DY (2015) Three-mode pulse-width modulation of a three-phase four-wire inverter. IET Power Electron 8(8):1483–1489
4. Li XF, Qu LL, Zhang B et al (2018) A simplified modulation strategy of nine-switch inverter to cut off half of switching modes. IEEE Access 6:7254–7261
5. Ezzine J, Haddad AH (1989) Controllability and observability of hybrid systems. Int J Control 49(6):2045–2055
6. Wang WB, Zhang B, Xie F (2018) A novel SVPWM for three-level NPC inverter based on m-mode controllability. IEEE Trans Ind Electron 65(8):6055–6065

Chapter 3
3-Mode SVPWM for Three-Phase Four-Wire Inverter

Three-phase four-wire inverter is one of the most common two-level inverters and is a representative in the inverters. In this chapter, according to the operation principle of the three-phase four-wire inverter, the switched linear system model of the three-phase four-wire inverter is established, and the condition of *m*-mode controllability is given by using the state controllability criterion of the inverter. It is concluded that three modes are the minimum operating modes to realize state controllability. The theoretical analysis, simulation, and experiment of 3-mode SVPWM are carried out.

3.1 Operating Principle of Three-Phase Four-Wire Inverter

The topology of the three-phase four-wire inverter is shown in Fig. 3.1. It can be seen that the three-phase four-wire inverter consists of three bridge arms and six power switches, and the load neutral point is connected with the DC side neutral point.

Since each bridge arm of the three-phase four-wire inverter has two switching states, there are eight operating modes for the inverter, which form eight basic voltage space vectors $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$,$\vec{V}_{s4}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$, $\vec{V}_{s7}$, and $\vec{V}_{s8}$, where $\vec{V}_{s7}$ and $\vec{V}_{s8}$ are the zero voltage space vectors. For the sake of simplicity, the operating mode is represented by the binary combination of the upper switch of each bridge arm, in which 1 for ON and 0 for OFF. Therefore, the switching state of the three-phase four-wire inverter, the corresponding voltage space vector and its binary representation are listed in Table 3.1.

The equivalent circuits of the eight operating modes are shown in Fig. 3.2. Six nonzero voltage space vectors $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$, and $\vec{V}_{s6}$ are uniformly symmetrically distributed on the complex plane, and divide the complex plane into six sectors I–VI, as shown in Fig. 3.3.

Any output voltage of the inverter can be synthesized by eight space voltage vectors. For example, if the desired voltage space vector $\vec{V}_{\text{ref}}$ locates in sector I, it

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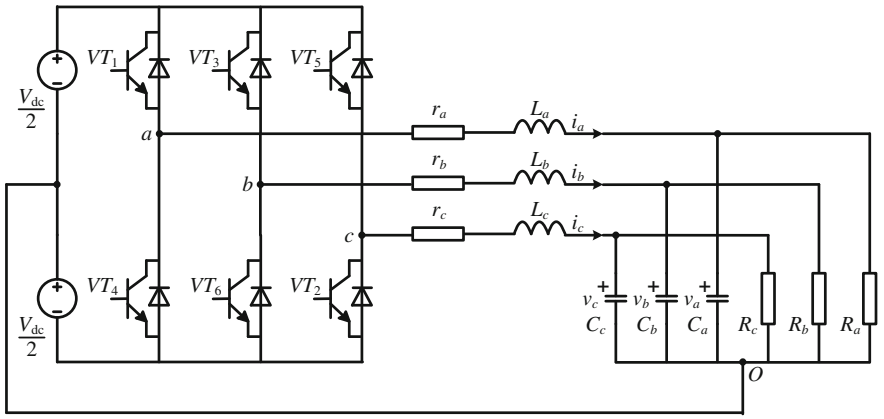


Fig. 3.1 Three-phase four-wire inverter

Table 3.1 Switching state, voltage space vector and binary representation of the three-phase four-wire inverter

Mode	VT_1	VT_3	VT_5	VT_4	VT_6	VT_2	Vector	Binary representation
1	ON	OFF	OFF	OFF	ON	ON	$\vec{V}_{s1}$	100
2	ON	ON	OFF	OFF	OFF	ON	$\vec{V}_{s2}$	110
3	OFF	ON	OFF	ON	OFF	ON	$\vec{V}_{s3}$	010
4	OFF	ON	ON	ON	OFF	OFF	$\vec{V}_{s4}$	011
5	OFF	OFF	ON	ON	ON	OFF	$\vec{V}_{s5}$	001
6	ON	OFF	ON	OFF	ON	OFF	$\vec{V}_{s6}$	101
7	OFF	OFF	OFF	ON	ON	ON	$\vec{V}_{s7}$	000
8	ON	ON	ON	OFF	OFF	OFF	$\vec{V}_{s8}$	111

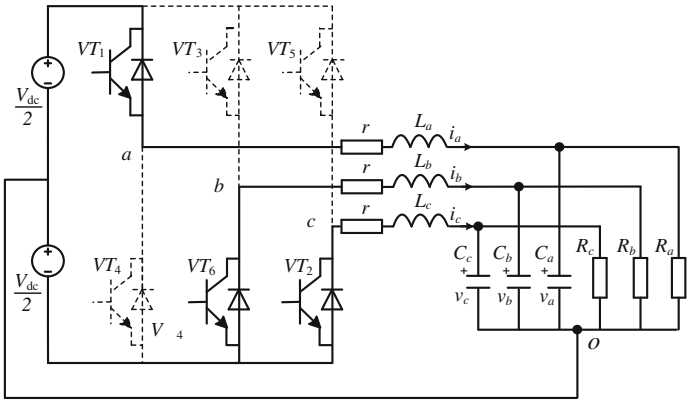
can be composed of $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s7}$, and $\vec{V}_{s8}$, according to the superposition principle of space vector [1, 2]. That is,

$$\vec{V}_{\text{ref}} T_s = T_{s1}\vec{V}_{s1} + T_{s2}\vec{V}_{s2} \tag{3.1}$$

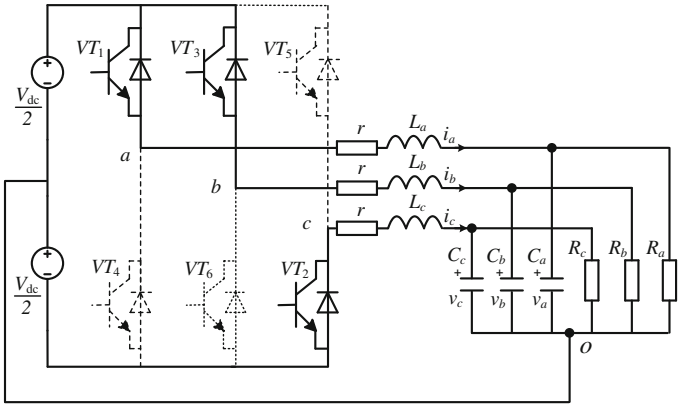
where T_s is the switching period; T_{s1} and T_{s2} are the duration time of $\vec{V}_{s1}$ and $\vec{V}_{s2}$, respectively. Then,

$$T_{s1} = \frac{V_{\text{ref}} \sin\left(\frac{\pi}{3} - \theta\right)}{V_{\text{sm}} \sin\frac{\pi}{3}} T_s = \frac{\sqrt{3} V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta + \frac{\pi}{6}\right) T_s \tag{3.2}$$

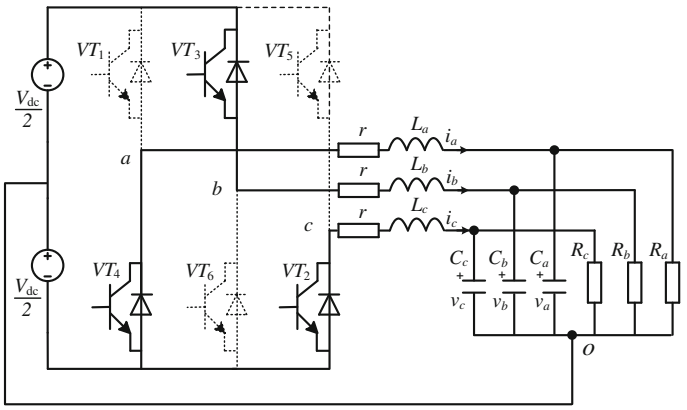
$$T_{s2} = \frac{V_{\text{ref}} \sin(\theta)}{V_{\text{sm}} \sin\frac{\pi}{3}} T_s = \frac{\sqrt{3} V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\frac{\pi}{2} - \theta\right) T_s \tag{3.3}$$



(a) Operating mode 1.

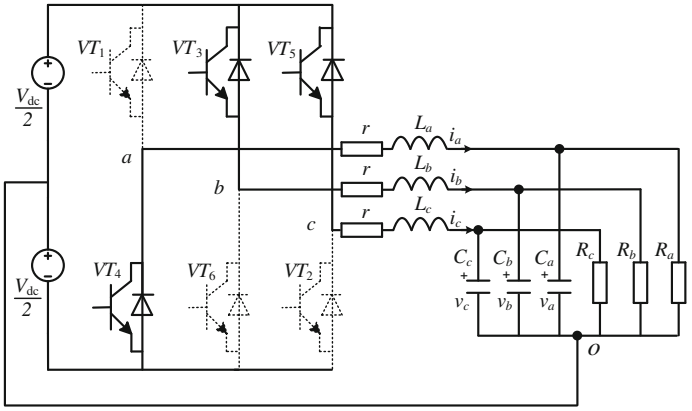


(b) Operating mode 2.

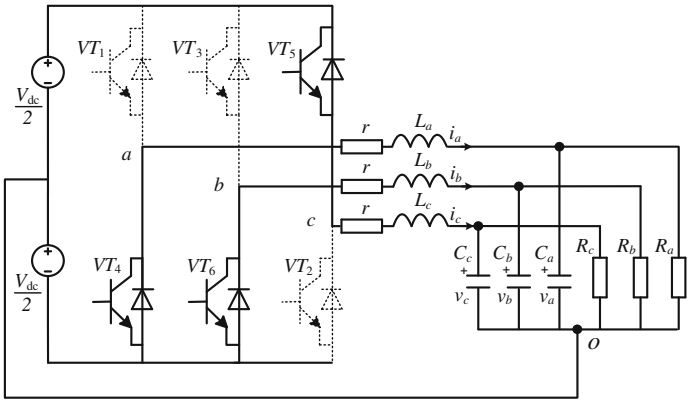


(c) Operating mode 3.

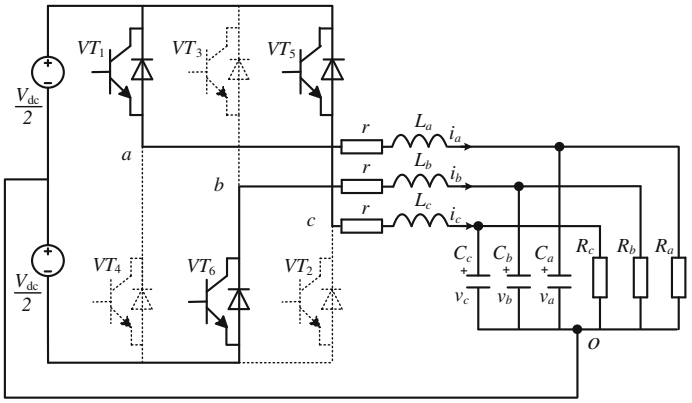
Fig. 3.2 Equivalent circuits of the three-phase four-line inverter



(d) Operating mode 4.

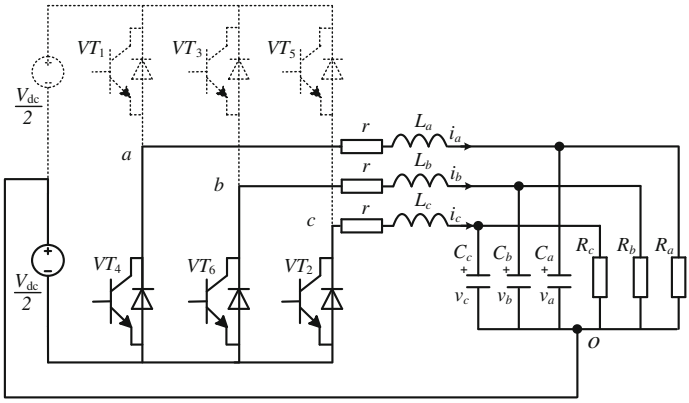


(e) Operating mode 5.

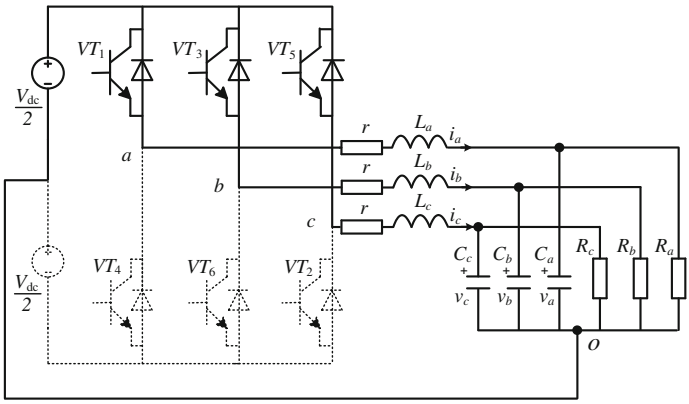


(f) Operating mode 6.

Fig. 3.2 (continued)



(g) Operating mode 7.



(h) Operating mode 8

Fig. 3.2 (continued)

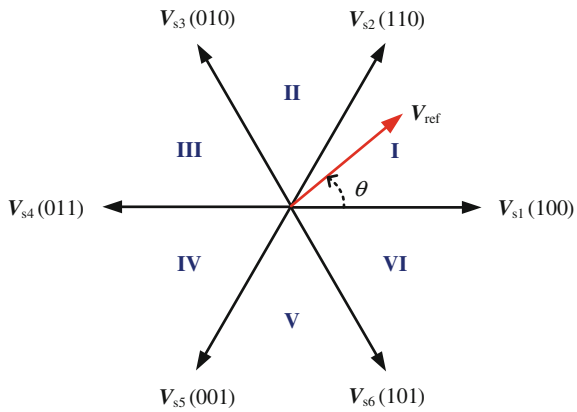


Fig. 3.3 Distribution of basic voltage space vectors

Table 3.2 Voltage space vector and its duration time of the three-phase four-wire inverter

Sector	Space vector	Duration time
I $\left(0 \le \theta < \frac{\pi}{3}\right)$	$\vec{V}_{s1}, \vec{V}_{s2}$	$T_{s1} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta + \frac{\pi}{6}\right)T_s$, $T_{s2} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{\pi}{2}\right)T_s$
II $\left(\frac{\pi}{3} \le \theta < \frac{2\pi}{3}\right)$	$\vec{V}_{s2}, \vec{V}_{s3}$	$T_{s2} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{\pi}{6}\right)T_s$, $T_{s3} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{5\pi}{6}\right)T_s$
III $\left(\frac{2\pi}{3} \le \theta < \pi\right)$	$\vec{V}_{s3}, \vec{V}_{s4}$	$T_{s3} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{\pi}{2}\right)T_s$, $T_{s4} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{7\pi}{6}\right)T_s$
IV $\left(\pi \le \theta < \frac{4\pi}{3}\right)$	$\vec{V}_{s4}, \vec{V}_{s5}$	$T_{s4} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{5\pi}{6}\right)T_s$, $T_{s5} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{3\pi}{2}\right)T_s$
V $\left(\frac{4\pi}{3} \le \theta < \frac{5\pi}{3}\right)$	$\vec{V}_{s5}, \vec{V}_{s6}$	$T_{s5} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{7\pi}{6}\right)T_s$, $T_{s6} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{11\pi}{6}\right)T_s$
VI $\left(\frac{5\pi}{3} \le \theta < 2\pi\right)$	$\vec{V}_{s6}, \vec{V}_{s1}$	$T_{s6} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{3\pi}{2}\right)T_s$, $T_{s1} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{\pi}{6}\right)T_s$

where V_{ref} is the amplitude of $\vec{V}_{\text{ref}}$; V_{sm} is the amplitude of the nonzero basic voltage space vector, and $V_{\text{sm}} = \frac{2}{3}V_{\text{dc}}$; $\theta = \omega t$ is the angle between $\vec{V}_{\text{ref}}$ and $\vec{V}_{s1}$, and ω is the rotation angle frequency of $\vec{V}_{\text{ref}}$, that is the angular frequency of the sinusoidal output voltage of the inverter.

In general, the sum of two duration time of the nonzero basic voltage space vectors cannot exceed one switching period, which means that $T_{s1} + T_{s2} < T_s$, then we have

$$\frac{T_{s1} + T_{s2}}{T_s} = \frac{\sqrt{3}V_{\text{ref}}}{V_{\text{dc}}} \cos\left(\theta - \frac{\pi}{6}\right) < 1, \theta \in \left(0, \frac{\pi}{6}\right) \tag{3.4}$$

The remaining operating time in one switching cycle ($T_s - T_{s1} - T_{s2}$) is taken by the combination of zero voltage space vectors $\vec{V}_{s7}$ and $\vec{V}_{s8}$. In addition, the maximum amplitude of $\vec{V}_{\text{ref}}$ can be derived from Eq. (3.4), that is

$$V_{\text{ref}} = \frac{\sqrt{3}}{3}V_{\text{dc}} \tag{3.5}$$

Therefore, the maximum line-to-line voltage amplitude of SVPWM is

$$V_{\text{ab}} = \sqrt{3}V_{\text{ref}} = V_{\text{dc}} \tag{3.6}$$

Table 3.2 lists the expressions of space voltage vectors and their corresponding duration time in each sector, which are used to generate any required space vector $\vec{V}_{\text{ref}}$.

3.2 Switched Linear System Model

The state variable is selected as $x = [i_a, i_b, i_c, v_a, v_b, v_c]^{\mathrm{T}}$, where i_a, i_b, i_c are the inductor currents of three-phase outputs, v_a, v_b, v_c are the capacitor voltages of the three-phase outputs. According to Fig. 3.1, the state equations of the inductor currents are listed as follows.

$$\begin{cases} L\dfrac{\mathrm{d}i_a}{\mathrm{d}t} = v_{\mathrm{ao}} - ri_a - v_a \\ L\dfrac{\mathrm{d}i_b}{\mathrm{d}t} = v_{\mathrm{bo}} - ri_b - v_b \\ L\dfrac{\mathrm{d}i_c}{\mathrm{d}t} = v_{\mathrm{co}} - ri_c - v_c \end{cases} \tag{3.7}$$

Similarly, the state equations of the capacitor voltages are given by

$$\begin{cases} C\dfrac{\mathrm{d}v_a}{\mathrm{d}t} = i_a - \dfrac{v_a}{R} \\ C\dfrac{\mathrm{d}v_b}{\mathrm{d}t} = i_b - \dfrac{v_b}{R} \\ C\dfrac{\mathrm{d}v_c}{\mathrm{d}t} = i_c - \dfrac{v_c}{R} \end{cases} \tag{3.8}$$

v_{ao}, v_{bo} and v_{co} in Eq. (3.7) are the voltages to the neutral point of the DC voltage source under different operating modes of the inverter, which are summarized in Table 3.3.

According to Eqs. (3.7) and (3.8), the switched linear system model similar to Eq. (2.1) with a switching variable $\sigma \in (1, 2, \ldots, i, \ldots, n)$ can be obtained as follows.

$$A_1 = \cdots = A_8 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} \end{bmatrix} \tag{3.9}$$

Table 3.3 Output voltage of the three-phase four-wire inverter under different operating modes

Mode	1	2	3	4	5	6	7	8
v_{ao}	$\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$
v_{bo}	$-\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$
v_{co}	$-\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$	$-\frac{V_{\mathrm{dc}}}{2}$	$\frac{V_{\mathrm{dc}}}{2}$

$$B_1 = \left[\begin{array}{ccccccc} \frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.10}$$

$$B_2 = \left[\begin{array}{ccccccc} \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.11}$$

$$B_3 = \left[\begin{array}{ccccccc} -\frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.12}$$

$$B_4 = \left[\begin{array}{ccccccc} -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.13}$$

$$B_5 = \left[\begin{array}{ccccccc} -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.14}$$

$$B_6 = \left[\begin{array}{ccccccc} \frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.15}$$

$$B_7 = \left[\begin{array}{ccccccc} \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.16}$$

$$B_8 = \left[\begin{array}{ccccccc} -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{3.17}$$

$$C_1 = \cdots = C_8 = \left[\begin{array}{cccccc} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{array}\right] \tag{3.18}$$

3.3 *m*-Mode Controllability

According to the Controllability Criterion 2.1 for power converter, the controllability analysis of the three-phase four-wire inverter will be carried out in this section. Since the operating modes 7 and 8 represent for the zero voltage vectors, the number of effective operating modes is 6, and the matrix corresponding to Eq. (2.6) is constructed as below.

$$\begin{aligned} &[B_1, \ldots, B_6, A_1B_1, \ldots, A_6B_1, \ldots, A_1B_6, \ldots, A_6B_6, \\ &\quad A_1^2B_1, \ldots, A_6A_1B_1, \ldots, A_1^2B_6, \ldots, A_6A_1B_6, \ldots, \\ &\quad A_1^5B_1, \ldots, A_6A_1^4B_1, \ldots, A_1A_6^4B_6, \ldots, A_6^5B_6] \end{aligned} \tag{3.19}$$

That is,

$$\left[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \ldots, \widehat{A}_5\right] \tag{3.20}$$

According to Eqs. (3.10)–(3.15), it is obvious that $\widehat{B} = [B_1, B_2, \ldots, B_6]$ is non-full rank, while $\widehat{A}_1 = \left[A_1\widehat{B}, A_2\widehat{B}, \ldots, A_n\widehat{B}\right]$ is a matrix of 6×36 dimensions, and

it is easy to calculate its rank equal to the number of state variables of the three-phase four-wire inverter [3], that is

$$\operatorname{rank}\left[\widehat{A}_1\right] = p = 6 \tag{3.21}$$

Therefore, there is no need to calculate the rank of $\widehat{A}_2$, $\widehat{A}_3$, $\widehat{A}_4$, and $\widehat{A}_5$ anymore. The rank of Eq. (3.20) is equal to the number of state variables of the three-phase four-wire inverter, it is concluded that the three-phase four-wire inverter is state-controllable.

Based on the state controllability of the three-phase four-wire inverter and Eq. (2.8), seven control variables can be formed when the number of the operating mode is $m = 3$, which is greater than the number of state variables of the converter. Therefore, the minimum number of the operating modes of the three-phase four-wire inverter is 3. According to Criterion 2.2, the symmetric operating modes 1, 3, 5 or 2, 4, 6 can be selected to form a new switching sequence, that is $\sigma \in (1, 3, 5)$ corresponding to $\sigma' \in (1, 2, 3)$ or $\sigma \in (2, 4, 6)$ corresponding to $\sigma' \in (1, 2, 3)$. According to Eq. (2.11), the rank of the three-phase four-wire inverter under the operating mode 1, 3, 5 or 2, 4, 6 can be calculated as below.

$$\begin{aligned}\operatorname{rank}\big[&B'_1, \ldots, B'_3, A'_1B'_1, \ldots, A'_1B'_3, \ldots, A'_3B'_1, \ldots, A'_3B'_3,\\ &A'^2_1B'_1 \ldots, A'^2_1B'_3, \ldots, A'_1A'_3B'_1, \ldots, A'_1A'_3B'_3, \ldots,\\ &A'_3A'_1B'_1, \ldots, A'_3A'_1B'_3, \ldots, A'^2_3B'_1, \ldots, A'^2_3B'_3\big] = 6\end{aligned} \tag{3.22}$$

where $A'_1 = A_1$, $A'_2 = A_3$, $A'_3 = A_5$, $B'_1 = B_1$, $B'_2 = B_3$, and $B'_3 = B_5$ for the switching sequence with operating modes 1, 3, 5; $A'_1 = A_2$, $A'_2 = A_4$, $A'_3 = A_6$, $B'_1 = B_2$, $B'_2 = B_4$, and $B'_3 = B_6$ for the switching sequence with operating modes 2, 4, 6. Equation (3.22) proves that the three-phase four-wire inverter is 3-mode controllable.

3.4 3-Mode SVPWM Strategy

According to the analysis results of *m*-mode controllability for the three-phase four-wire inverter, the three-phase four-wire inverter is controllable by using three operating modes, and 3 is the minimum number of operating modes that can realize state-controllable. The synthesis voltage vector can be formed by three basic space voltage vectors corresponding to these three operating modes, and the SVPWM can be realized. In order to analyze the principle of the 3-mode SVPWM, the 3-mode SVPWM consisting of operating modes 1, 3 and 5 is called the 3-mode SVPWM I, and that consisting of operating modes 2, 4, and 6 is called the 3-mode SVPWM II.

3.4.1 3-Mode SVPWM I

The basic voltage space vectors $\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$ corresponding to the operating modes 1, 3 and 5 form a complex plane as shown in Fig. 3.4, in which six sectors of conventional SVPWM are reduced to three sectors, that is, sectors I and II, sectors III and IV, sectors V and VI are combined into one new sector, respectively. In the 3-mode SVPWM I, the required output voltage vector $\vec{V}_{\text{ref}}$ is synthesized by $\vec{V}_{s1}$ and $\vec{V}_{s3}$, or $\vec{V}_{s3}$ and $\vec{V}_{s5}$, or $\vec{V}_{s5}$ and $\vec{V}_{s1}$, according to the parallelogram law of vector superposition, and rotates in a circular path to obtain the three-phase sinusoidal output voltage.

The specific synthesis process of $\vec{V}_{\text{ref}}$ is introduced as follows. First, the sector in which $\vec{V}_{ref}$ is the sector should be determined. In the stationary coordinate $\alpha - \beta$, the components of $\vec{V}_{\text{ref}}$ on the $\alpha - \beta$ two-phase coordinate arises are $\vec{V}_{\text{ref}\alpha}$ and $\vec{V}_{\text{ref}\beta}$, respectively. Then, the sector in which $\vec{V}_{\text{ref}}$ belongs to is determined by

$$\begin{aligned} N = \text{sign}\left(V_{\text{ref}\beta}\right) + 2 \times \text{sign}\left(V_{\text{ref}\alpha} \sin\frac{\pi}{3} - V_{\text{ref}\beta} \sin\frac{\pi}{6}\right) \\ - 4 \times \text{sign}\left(V_{\text{ref}\alpha} \sin\frac{\pi}{3} + V_{\text{ref}\beta} \sin\frac{\pi}{6}\right) \end{aligned} \tag{3.23}$$

where $V_{\text{ref}\alpha}$ and $V_{\text{ref}\beta}$ are the magnitudes of $\vec{V}_{\text{ref}\alpha}$ and $\vec{V}_{\text{ref}\beta}$, respectively.

When $N = 1$ or 3, $\vec{V}_{\text{ref}}$ locates in sector I or II and can be synthesized by $\vec{V}_{s1}$ and $\vec{V}_{s3}$, as shown in Fig. 3.5a. When $N = 4$ or 5, $\vec{V}_{\text{ref}}$ locates in sector III or IV and can be synthesized by $\vec{V}_{s3}$ and $\vec{V}_{s5}$, as shown in Fig. 3.5b. When $N = 2$ or 6, $\vec{V}_{\text{ref}}$ locates in sector V or VI and can be synthesized by $\vec{V}_{s5}$ and $\vec{V}_{s1}$, as shown in Fig. 3.5c.

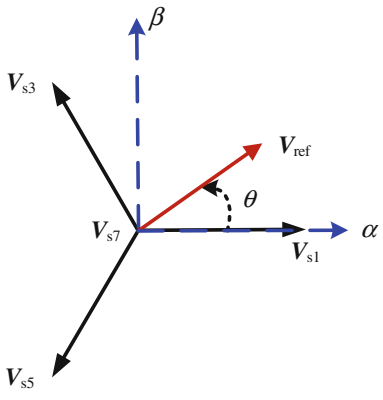
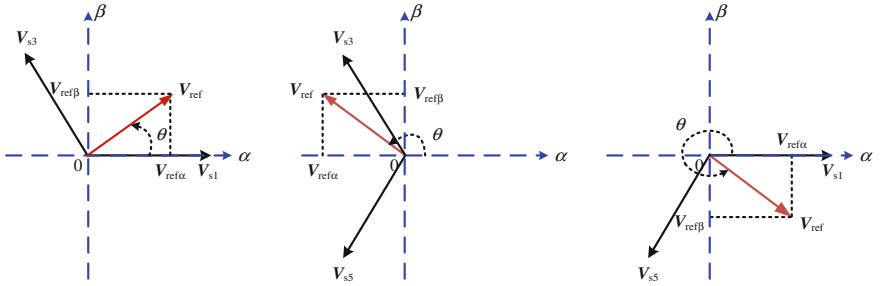


Fig. 3.4 Voltage vector distribution of 3-mode SVPWM I



(a) Sector I, II **(b)** Sector III, IV **(c)** Sector V, VI

Fig. 3.5 Voltage vector construction of 3-mode SVPWM I

when $\vec{V}_{\text{ref}}$ locates in sectors I and II, the relationship among $\vec{V}_{\text{ref}}$, $\vec{V}_{s1}$ and $\vec{V}_{s3}$ satisfies with the following equation:

$$V_{\text{ref}} T_s = V_{s1} T_{s1} + V_{s3} T_{s3} \tag{3.24}$$

where V_{ref}, V_{s1} and V_{s3} are the magnitudes of $\vec{V}_{\text{ref}}$, $\vec{V}_{s1}$ and $\vec{V}_{s3}$, respectively; T_s, T_{s1}, T_{s3} are the duration of the switching cycle, $\vec{V}_{s1}$ and $\vec{V}_{s3}$, respectively.

According to Fig. 3.5a, Eq. (3.24) can be rewritten to

$$\begin{aligned}\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} T_s &= V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos 0 \\ \sin 0 \end{bmatrix} T_{s1} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos\frac{2\pi}{3} \\ \sin\frac{2\pi}{3} \end{bmatrix} T_{s3} \\ &= \frac{2}{3} V_{\text{dc}} \begin{bmatrix} 1 \\ 0 \end{bmatrix} T_{s1} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s3} \end{aligned} \tag{3.25}$$

where θ is the angle between $\vec{V}_{\text{ref}}$ and the α-axis.

Based on Eq. (3.25), the duration times of $\vec{V}_{s1}$ and $\vec{V}_{s3}$ can be determined by

$$T_{s1} = \frac{1}{V_{\text{dc}}} \left(\frac{3}{2} V_{\text{ref}\alpha} + \frac{\sqrt{3}}{2} V_{\text{ref}\beta} \right) T_s \tag{3.26}$$

$$T_{s3} = \sqrt{3} \frac{V_{\text{vef}\beta}}{V_{\text{dc}}} T_s \tag{3.27}$$

Considering the zero voltage space vector $\vec{V}_{s7}$, then we have

$$T_{s7} = T_s - T_{s1} - T_{s3} \tag{3.28}$$

Similarly, when $\vec{V}_{\text{ref}}$ locates in sectors III and IV, and is synthesized by $\vec{V}_{s3}$ and $\vec{V}_{s5}$, the duration times of $\vec{V}_{s3}$, $\vec{V}_{s5}$ and $\vec{V}_{s7}$ are given by

$$T_{s3} = \frac{1}{V_{\text{dc}}}\left(\frac{3}{2}V_{\text{ref}\alpha} + \frac{\sqrt{3}}{2}V_{\text{ref}\beta}\right)T_s \tag{3.29}$$

$$T_{s5} = -\frac{1}{V_{\text{dc}}}\left(\frac{3}{2}V_{\text{ref}\alpha} + \frac{\sqrt{3}}{2}V_{\text{ref}\beta}\right)T_s \tag{3.30}$$

$$T_{s7} = T_s - T_{s3} - T_{s5} \tag{3.31}$$

When $\vec{V}_{\text{ref}}$ is located in sectors V and VI, and is synthesized by $\vec{V}_{s5}$ and $\vec{V}_{s1}$, the duration times of $\vec{V}_{s5}$, $\vec{V}_{s1}$ and $\vec{V}_{s7}$ are given by

$$T_{s5} = \frac{1}{V_{\text{dc}}}\left(\frac{3}{2}V_{\text{ref}\alpha} - \frac{\sqrt{3}}{2}V_{\text{ref}\beta}\right)T_s \tag{3.32}$$

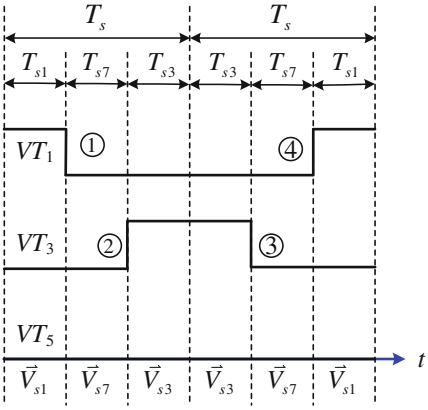
$$T_{s1} = -\sqrt{3}\frac{V_{\text{ref}\beta}}{V_{\text{dc}}}T_s \tag{3.33}$$

$$T_{s7} = T_s - T_{s5} - T_{s1} \tag{3.34}$$

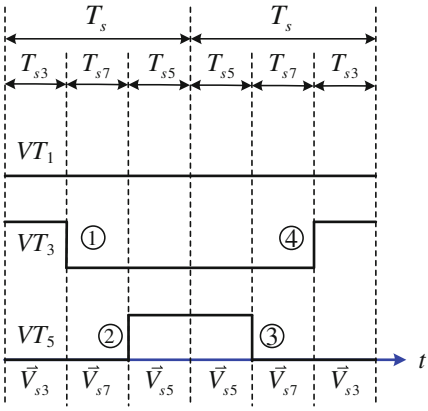
Assume that the synchronous modulation is used, that is, the modulation ratio keeps constant, and only one switching device is switched ON or OFF every time. The switching sequences of 3-mode SVPWM I are shown in Fig. 3.6. When $\vec{V}_{\text{ref}}$ locates in sector I or II, it can be seen from Fig. 3.6a that the operating mode 1 corresponding to $\vec{V}_{s1}$ starts to work at the end of the last cycle, and continues to work for a time of T_{s1}; then the operating mode is switched from mode 1 to mode 7 which is corresponding to the zero voltage vector $\vec{V}_{s7}$ and lasts for a time of T_{s7}; next, the operating mode is switched to mode 3 corresponding to $\vec{V}_{s3}$ and works for a time of T_{s3}, and the first cycle ends. In order to reduce the number of switching times, in the second cycle, the operating mode 3 continues to work for a time of T_{s3}, then switches to mode 7 corresponding to the zero voltage vector $\vec{V}_{s7}$ and works for a time of T_{s7}, finally switches to mode 1 and continues for a time of T_{s1}. Then the second cycle ends. Similarly, when $\vec{V}_{\text{ref}}$ locates in sector III or IV, the corresponding switching sequence is shown in Fig. 3.6b. In addition, the switching sequence corresponding to $\vec{V}_{\text{ref}}$ that is located in sector V or VI is shown in Fig. 3.6c.

Table 3.4 shows the switching sequence of the three-phase four-wire inverter according to Fig. 3.6, as well as that of the conventional SVPWM. For one sector in the 3-mode SVPWM I, for example in Fig. 3.6a, the upper switch VT_1 of phase a is turned on and off once within two switching cycles, the upper switch VT_3 of phase b is turned on and off once, while the upper switch VT_5 of phase c is kept off.

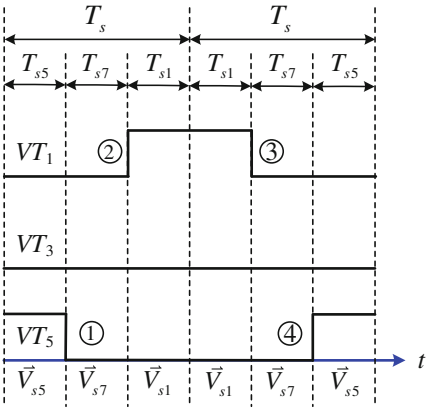
Fig. 3.6 Switching sequences of 3-mode SVPWM I



(a) Sectors I and II.



(b) Sectors III and IV.



(c) Sectors V and VI.

Table 3.4 Switching sequences of conventional SVPWM and 3-mode SVPWM I

Sector	Conventional SVPWM	Switching times	3-mode SVPWM I	Switching times
I	000-100-110-111-110-100-000-100-110-111-110-100-000	12	100-000-010-000-100	4
II	000-010-110-111-110-010-000-010-110-111-110-010-000	12	100-000-010-000-100	4
III	000-010-011-111-011-010-000-010-011-111-011-010-000	12	010-000-001-000-010	4
IV	000-001-011-111-011-001-000-001-011-111-011-001-000	12	010-000-001-000-010	4
V	000-001-101-111-101-001-000-001-101-111-101-001-000	12	001-000-100-000-001	4
VI	000-100-101-111-101-100-000-100-101-111-101-100-000	12	001-000-100-000-001	4
Total		72		24

Similarly, as shown in Fig. 3.6b, VT_1 is kept off, while both VT_3 and VT_5 are turned on and off once within two switching cycles. In Fig. 3.6c, VT_3 is kept off, while both VT_1 and VT_5 are turned on and off once within two switching cycles. As a result, only four switching times are necessary in each sector when the 3-mode SVPWM I is used. However, the switches need to be switched 12 times in each sector when the conventional SVPWM is used. Therefore, the equivalent switching frequency of the 3-mode SVPWM I is reduced by 2/3 compared with the conventional SVPWM control.

In addition, the inversion design of the switching sequence in different cycle is beneficial to eliminate the voltage spikes generated during the operation mode switching. Taking the switching sequence in sector I as an example, the switching sequence is 100-000-010 in the first or odd switching cycle and is reversed to 010-000-100 in the second or even switching cycle. This design makes the operating mode at the end of the previous cycle be the same as that at the beginning of the next cycle. That is, only one bridge arm is involved during each switching process, in that way the generation of voltage spikes during the commutation process will be reduced.

3.4.2 3-Mode SVPWM II

The 3-mode SVPWM II includes operating modes 2, 4, and 6, and the corresponding basic voltage space vectors $\vec{V}_{s2}$, $\vec{V}_{s4}$, and $\vec{V}_{s6}$ form a complex plane as shown in Fig. 3.7. The 3-mode SVPWM II also reduces the six sectors of conventional SVPWM to three sectors, in which sectors II and III are combined into one sector, sectors IV and V are combined into one sector, and sectors VI and I are combined into one sector.

$\vec{V}_{\text{ref}}$ can be synthesized by $\vec{V}_{s2}$ and $\vec{V}_{s4}$ when it locates in sector II or III, by $\vec{V}_{s4}$ and $\vec{V}_{s6}$ in sector IV or V, or by $\vec{V}_{s6}$ and $\vec{V}_{s2}$ in sector VI or I. The corresponding

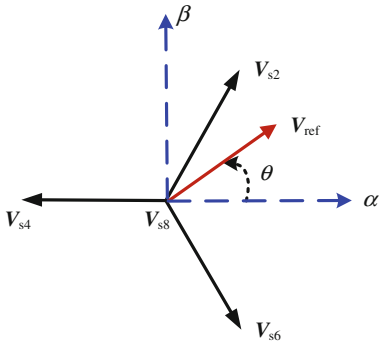


Fig. 3.7 Voltage vector distribution of 3-mode SVPWM II

Table 3.5 Switching sequences of 3-mode SVPWM II

Sector	3-mode SVPWM II	Switching times
I	110-111-101-111-110	4
II	110-111-011-111-110	4
III	110-111-011-111-110	4
IV	011-111-101-111-011	4
V	011-111-101-111-011	4
VI	110-111-101-111-110	4
Total		24

switching sequences are shown in Fig. 3.8, and the duration time of each basic voltage vector can be obtained by the similar way in the 3-mode SVPWM I.

Table 3.5 lists the switching sequences of the 3-mode SVPWM II corresponding to Fig. 3.7 for two switching cycles. Similar to the 3-mode SVPWM I, only three operating modes are used, then the number of switching times are reduced. As a result, the equivalent switching frequency is only one-third of the conventional SVPWM.

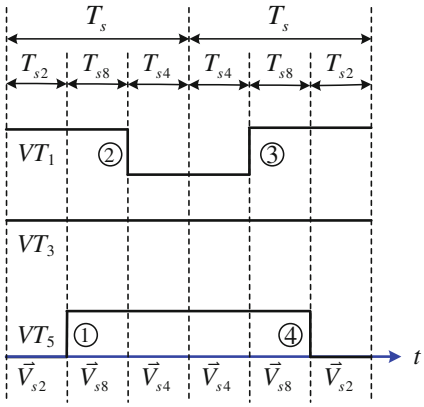
3.5 Characteristic Analysis

3.5.1 Output Voltage

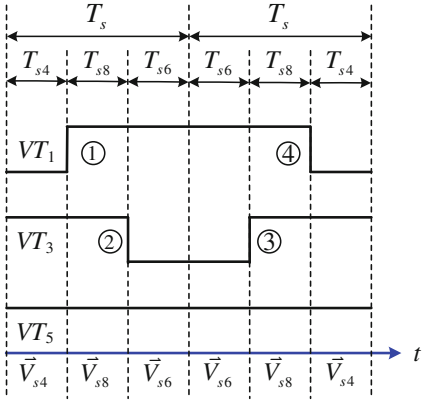
Referring to Fig. 3.1, the parameters of the three-phase four-wire inverter are set as follows: the filter inductor $L = 4$ mH, the filter capacitor $C = 6.8$ μF, the line equivalent resistor $r = 0.5\ \Omega$, the carrier frequency $f_c = 10$ kHz, the output frequency $f_r = 50$ Hz, and the RMS value of the output line voltage is 110 V.

Figure 3.9 shows the simulation waveforms of the output voltage under the 3-mode SVPWMs I and II. Figure 3.9a and b show the phase voltage waveforms of the 3-mode SVPWMs I and II, respectively. It can be seen that the phase voltage waveforms

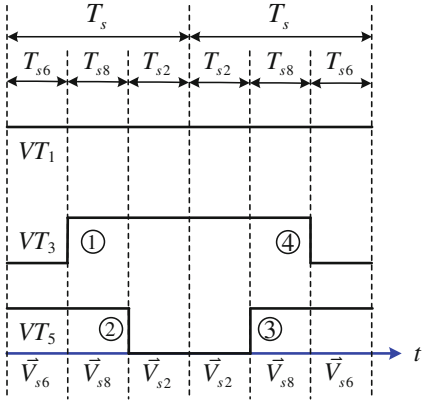
Fig. 3.8 Switching sequences of 3-mode SVPWM II



(a) Sectors II and III.



(b) Sectors IV and V.



(c) Sectors VI and I.

of the 3-mode SVPWMs I and II are opposite, but the line voltage waveforms are the same.

Figure 3.10 shows the experimental waveforms of 3-mode SVPWM I and II. Comparing to the simulation waveforms in Fig. 3.9, the experimental waveforms are identical to the simulation ones, which demonstrate the validity and correctness of 3-mode SVPWM.

3.5.2 Switching Frequency

Figure 3.11 shows the number of switching of the switching device VT_1 within one output fundamental cycle, and the results of conventional SVPWM, 3-mode SVPWM I and II at the same carrier frequency 10 kHz are illustrated in Fig. 3.11a–c, respectively. It is obvious from Fig. 3.11 that the switching times is 200 in the conventional SVPWM, but only 67 in 3-mode SVPWM. Therefore, the equivalent switching frequency of 3-mode SVPWM is only 1/3 of that of the conventional SVPWM.

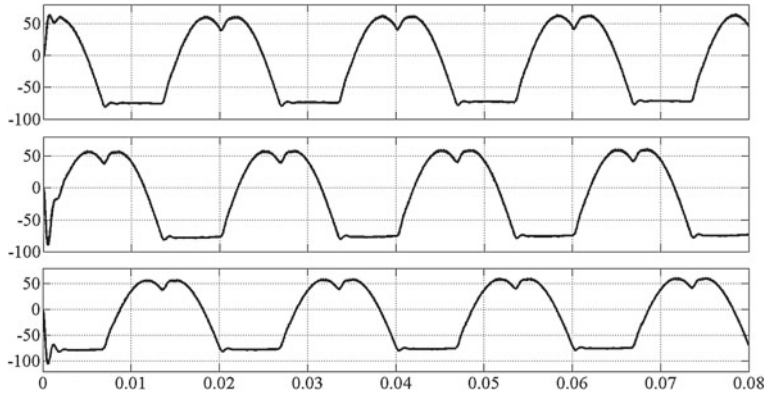
3.5.3 Harmonic Contents and Efficiency

Figure 3.12a and b show the spectrums of the output line voltage under the conventional SVPWM and the 3-mode SVPWM at the same carrier frequency, respectively. It can be seen from Fig. that the high-frequency harmonics of the line voltage and the total harmonic distortion (THD) of the 3-mode SVPWM are slightly higher than those of the conventional SVPWM, but the equivalent switching frequency of the 3-mode SVPWM is only one-third of that of the conventional SVPWM. If the carrier frequency of the 3-mode SVPWM is increased to 30 kHz, then the corresponding switching frequency is the same as that of the conventional SVPWM switching frequency, and the THD of the line voltage will be lower than that of the conventional SVWPM.

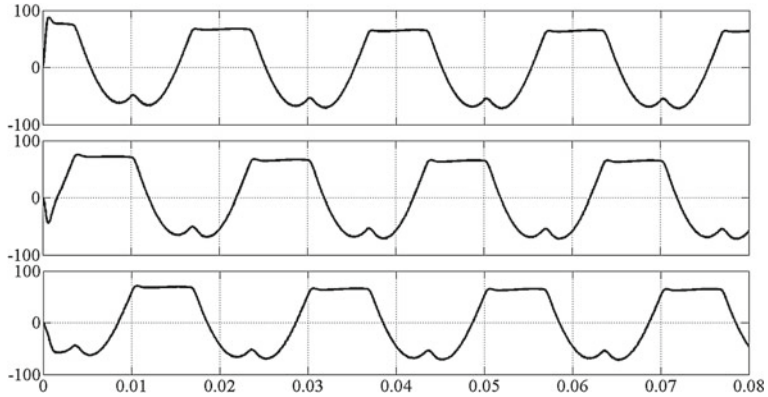
The efficiency curves of the three-phase four-line inverter under the conventional SVPWM and the 3-mode SVPWM are given in Fig. 3.13. With the same output power and the same power switching devices, the 3-mode SVPWM inverter is significantly more efficient due to fewer switching times.

3.5.4 Improved 3-Mode SVPWM

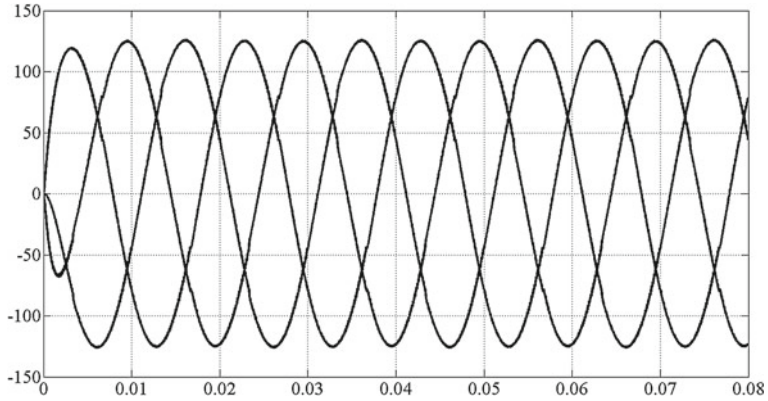
There is a common problem existed in the 3-mode SVPWMs I and II, that is, the current flowing through the upper and lower switching devices of the same bridge arm is unbalanced. Taking the 3-mode SVPWM I as an example, in sectors I and



(a) Phase voltages of *3*-mode SVPWM I.

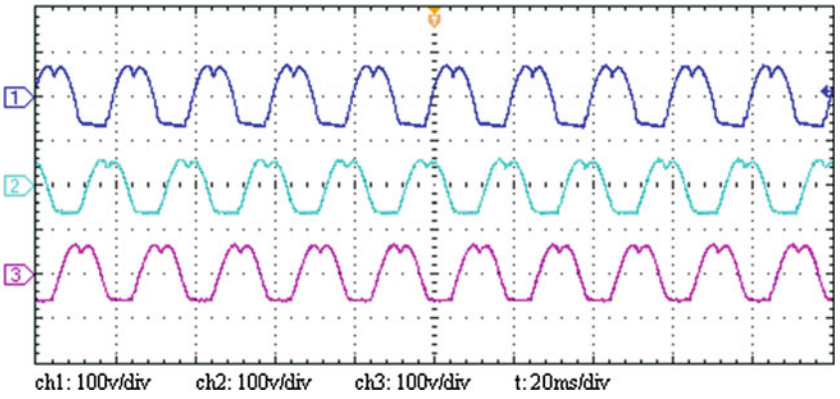


(b) Phase voltages of *3*-mode SVPWM II.

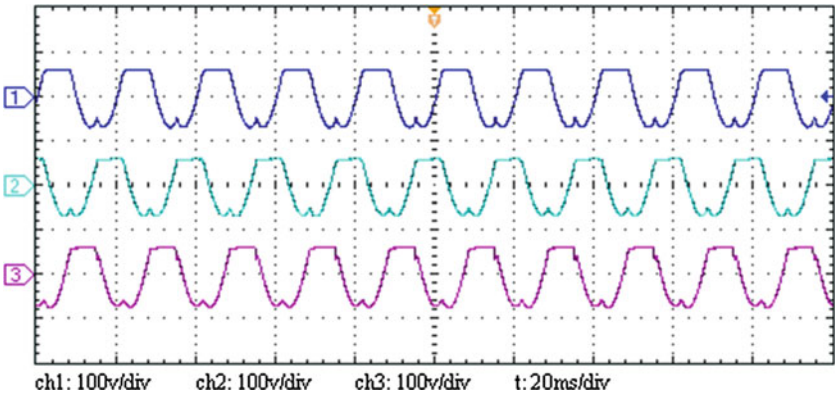


(c) Line voltages of *3*-mode SVPWM I.

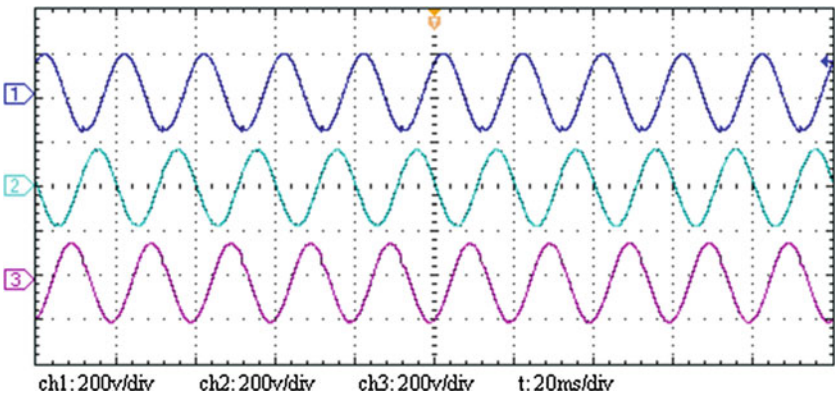
Fig. 3.9 Simulation waveforms of the output voltages with 3-mode SVPWM



(a) Phase voltages of *3*-mode SVPWM I.

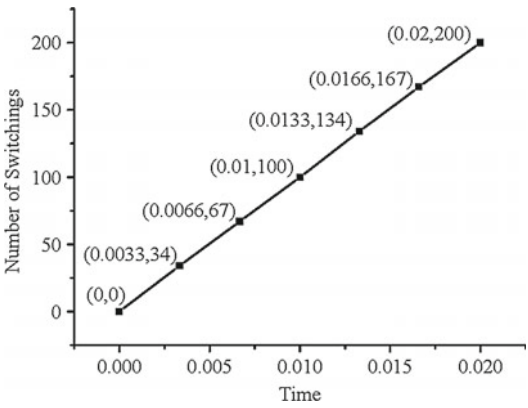


(b) Phase voltages of *3*-mode SVPWM II.

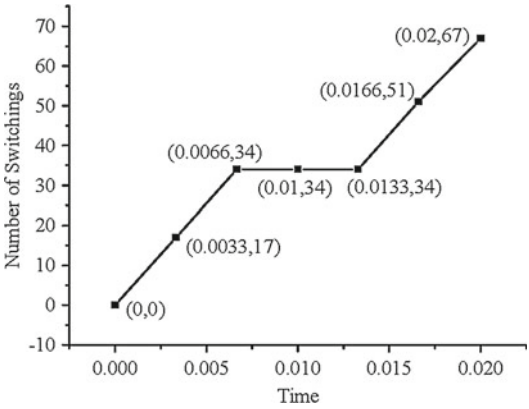


(c) Line voltages of *3*-mode SVPWM I.

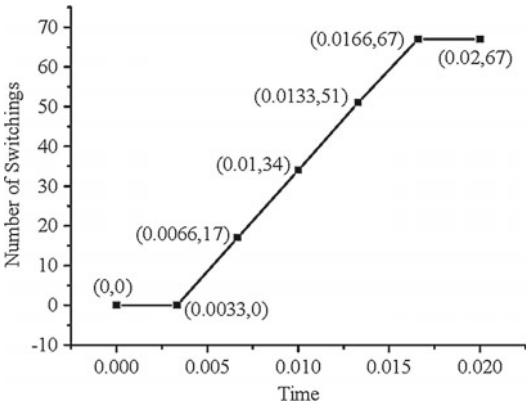
Fig. 3.10 Experimental waveforms of the output voltage with 3-mode SVPWM



(a) Conventional SVPWM.

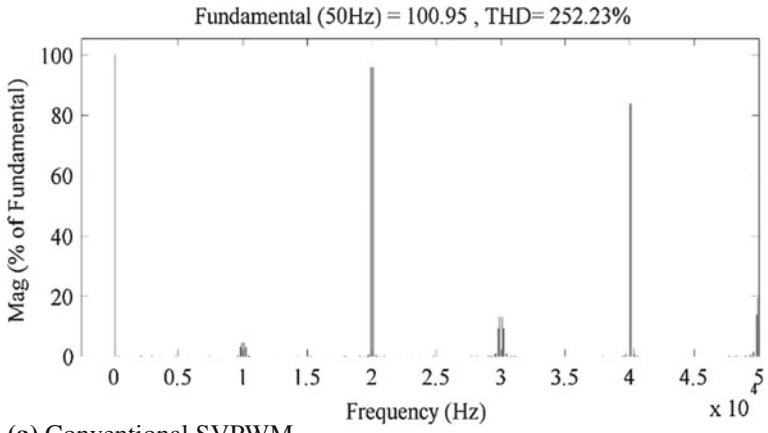


(b) *3*-mode SVPWM I.

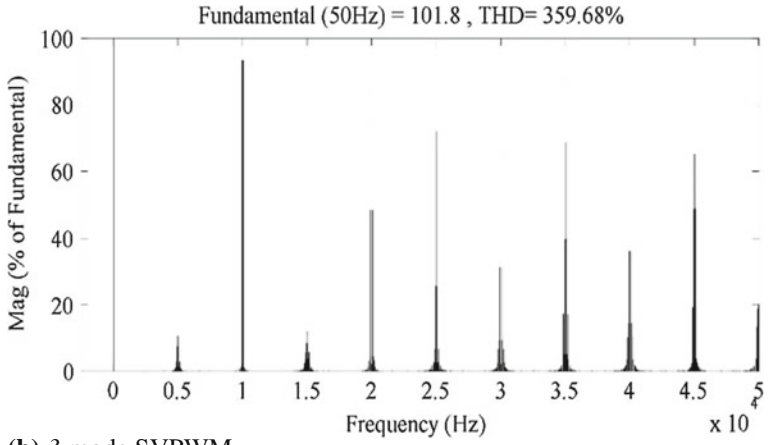


(c) *3*-mode SVPWM II.

Fig. 3.11 Number of switching times under different SVPWMs



(a) Conventional SVPWM.



(b) *3*-mode SVPWM.

Fig. 3.12 Output line voltage spectrums of different SVPWMs

VI, the switching device VT_1 is kept on while VT_4 remains off, but in the other four sectors, VT_1 and VT_4 are alternately turned on and off. It is obvious that the time that the current flows through VT_1 is longer than that passing through VT_4. In order to solve the current unbalance problem, different kinds of switching devices should be considered in the system. For example, an IGBT with a low on-resistance is preferred for the switch with a small number of switching times and a long turn-on time, while a MOSFET with a high switching frequency is selected for the switch with a large number of switching times and a short turn-on time.

In addition, a hybrid 3-mode SVPWM (or 3-mode SVPMW III) as listed in Table 3.6 has been designed to solve the current unbalance problem of the switching

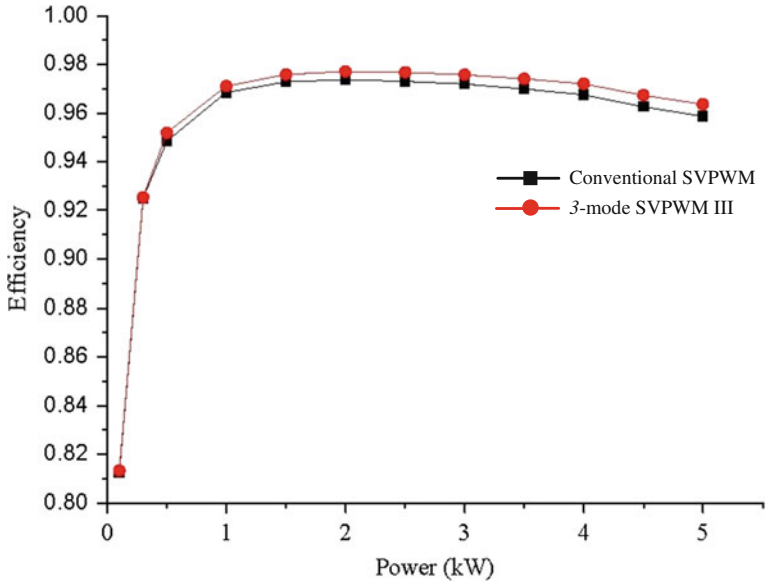


Fig. 3.13 Efficiencies of conventional SVPWM and 3-mode SVPWM III

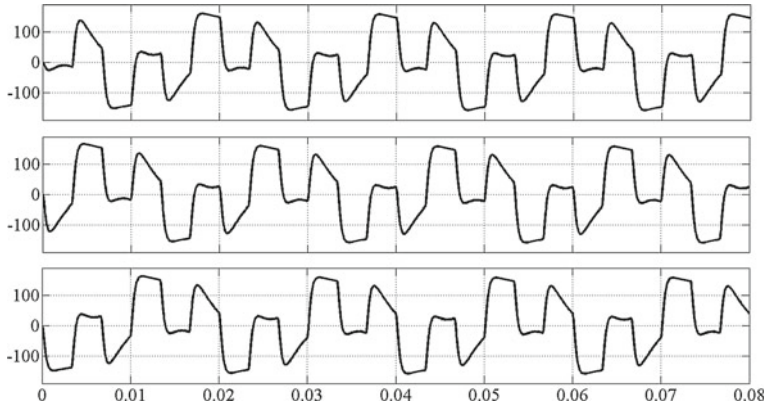
Table 3.6 Switching sequence of hybrid 3-mode SVPWM (3-mode SVPWM III)

Sector	Switching sequence	Switching times	Hybrid 3-mode SVPWM
I	100-000-010-000-100	4	3-mode SVPWM I
II	110-111-011-111-110	4	3-mode SVPWM II
III	010-000-001-000-010	4	3-mode SVPWM I
IV	011-111-101-111-011	4	3-mode SVPWM II
V	001-000-100-000-001	4	3-mode SVPWM I
VI	110-111-101-111-110	4	3-mode SVPWM II
Total		24	

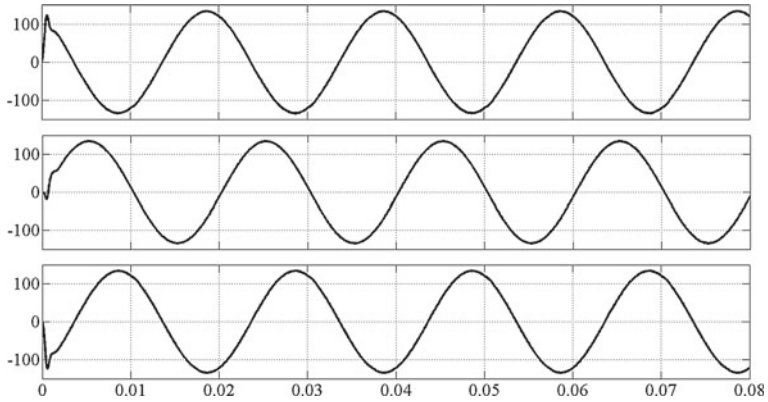
devices. From Table 3.6, the 3-mode SVPWM III alternates the switching sequence of the 3-mode SVPWMs I and II in different sectors, which can effectively balance the current carried by the switching devices.

Referring to Tables 3.4 and 3.5, the hybrid 3-mode SVPWM listed in Table 3.6 combines the switching sequences of the 3-mode SVPWMs I and II. Comparing with the 3-mode SVPWMs I and II, the hybrid 3-mode SVPWM or the 3-mode SVPWM III can not only balance the currents of the switching devices but also keep the switching frequency same to that of the 3-mode SVPWM I or II.

Figures 3.14 and 3.15 are the simulation and experimental waveforms of the output voltage under the 3-mode SVPWM III, respectively. Difference from the 3-mode SVPWMs I and II, the output phase voltage of the 3-mode SVPWM III is positive and negative symmetry, but the switching frequency of the 3-mode SVPWM III is the same as those of the 3-mode SVPWMs I and II, as shown in Fig. 3.16.



(a) Phase voltages.



(b) Line voltages.

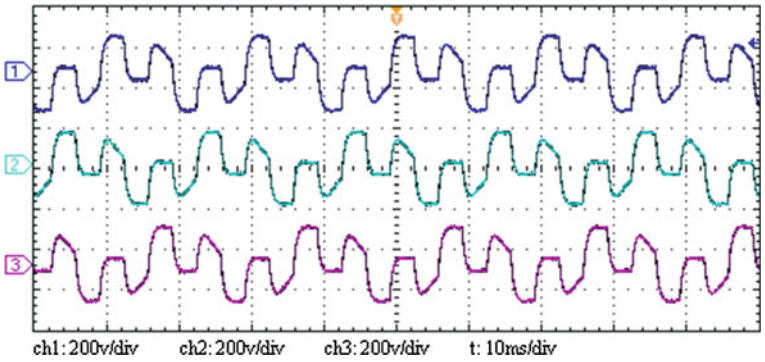
Fig. 3.14 Simulation waveforms of the output voltages with 3-mode SVPWM III

3.5.5 Application on Three-Phase Three-Wire Inverter

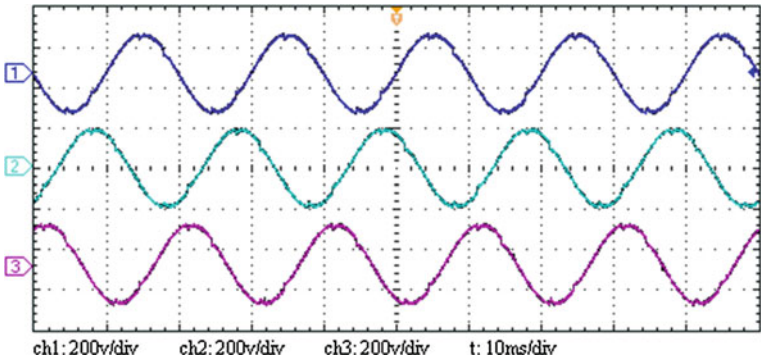
For the three-phase three-wire inverter, since the voltage and current of one phase can be derived from the other two phases, the converter has only four independent state variables, but there are still eight operating modes.

According to the converter controllability Criterion 2.1, the controllability analysis of the three-phase three-wire inverter is also carried out based on its switched linear system model. Corresponding to Eq. (2.6), we have

$$\begin{aligned}&\operatorname{rank}[B_1, \ldots, B_6, A_1B_1, \ldots, A_6B_1, \ldots, A_1B_6, \ldots, A_6B_6,\\ &\quad A_1^2B_1, \ldots, A_6A_1B_1, \ldots, A_1^2B_6, \ldots, A_6A_1B_6, \ldots,\\ &\quad A_1^5B_1, \ldots, A_6A_1^4B_1, \ldots, A_1A_6^4B_6, \ldots, A_6^5B_6] = 4\end{aligned} \tag{3.35}$$



(a) Phase voltages.



(b) Line voltages.

Fig. 3.15 Experimental waveforms of output voltages with 3-mode SVPWM III

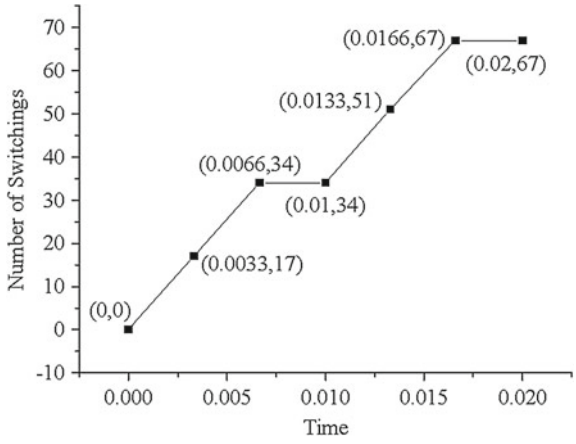
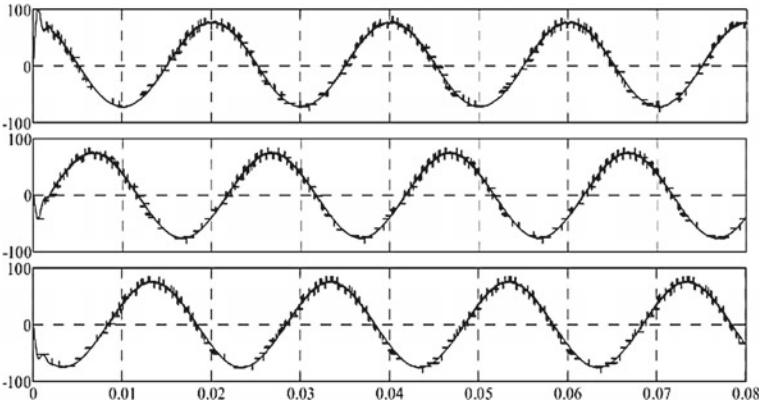
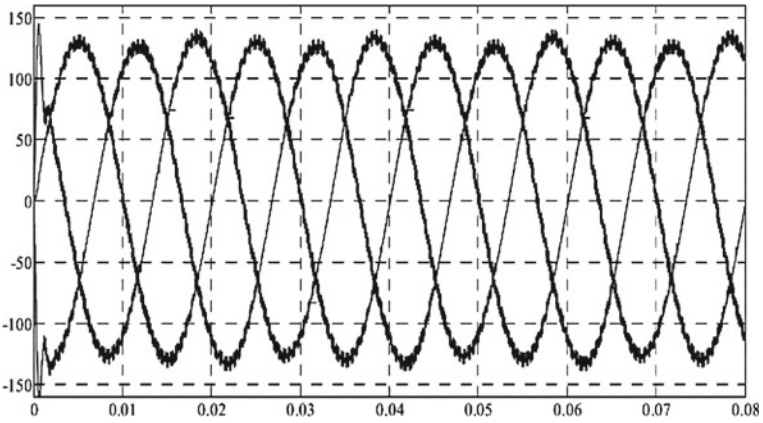


Fig. 3.16 Switching times of 3-mode SVPWM III



(a) Phase voltages



(b) Line voltages

Fig. 3.17 Simulation waveforms of the three-phase three-wire inverter with 3-mode SVPWM I

Equation (3.35) shows that the three-phase three-wire inverter is state-controllable.

Similar to the three-phase four-wire inverter, the symmetrical operating modes 1, 3, and 5 (or 2, 4, and 6) are selected to form a new switching sequence to realize the 3-mode SVPWM. Figure 3.17 shows the simulation waveforms of the output voltage of the three-phase three-wire inverter with the 3-mode SVPWM I. It can be seen from Fig. 3.17 that both the phase and the line voltages of the three-phase three-wire inverter are sinusoidal waveforms.

The number of switching times of the three-phase three-wire inverter with the 3-mode SVPWM in one fundamental cycle is provided in Fig. 3.18. It is the same as that of the three-phase four-wire inverter, which indicates that the number of switching times does not change as the inverter connection mode changes.

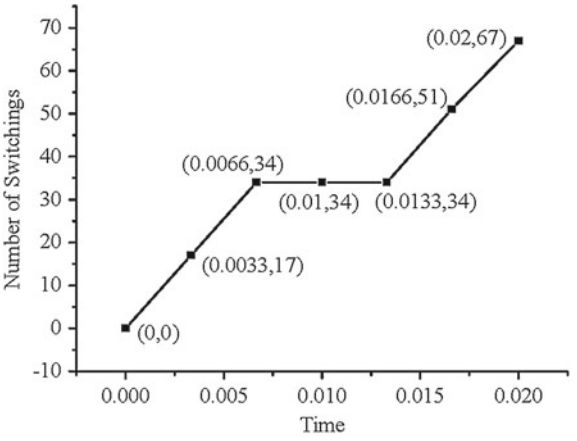


Fig. 3.18 Switching times of the three-phase three-wire inverter with 3-mode SVPWM

3.6 Summary

This chapter analyzes the *m*-mode controllability of the three-phase four-wire inverter and proves that three modes are the minimum controllable condition. Therefore, two kinds of 3-mode SVPWM methods have been proposed by using different group of basic voltage vectors. Then, the synthesis method of the voltage space vector and the corresponding switching sequence are analyzed systematically. Simulation and experimental results show that the 3-mode SVPWM actually has only three sectors, which is half of the conventional SVPWM, which reduces the calculation time of switching time. Consequently, the equivalent switching frequency of the switching component is reduced to 1/3, which will significantly improve the efficiency of the inverter. The 3-mode SVPWM can be formed in a variety of ways and is also suitable for the three-phase three-wire inverter.

References

1. Grant DA, Stevens M, Houldsworth JA (1985) The effect of word length on the harmonic content of microprocessor-based PWM waveform generators. IEEE Trans Ind Appl IA-21(1):218–225
2. Van Der Broeck HW, Skudelny HC, Stanke GV (1988) Analysis and realization of a pulsewidth modulator based on voltage space vectors. IEEE Trans Ind Appl 24(1):142–150
3. Li X, Zhang B, Qiu D (2015) Three-mode pulse-width modulation of a three-phase four-wire inverter. IET Power Electron 8(8):1483–1489

Chapter 4
4-Mode SVPWM for Three-Phase Four-Wire Inverter

The previous chapter introduced the *m*-mode controllability and the 3-mode SVPWM characteristics of the three-phase four-wire inverter. According to the definition of the *m*-mode controllability, the 3-mode SVPWM is only one kind of many *m*-mode SVPWMs, and is the one with the least number of modes. In order to illustrate the diversity and selectivity of the *m*-mode SVPWM, this chapter will analyze the characteristics of the 4-mode SVPWM. Therefore, different modes of SVPWM can be provided for different applications. Furthermore, the geometric meaning of the *m*-mode SVPWM will be discussed, and the possible *m*-mode SVPWM method for the three-phase four-wire inverter will be investigated.

4.1 4-Mode Controllability

According to the criterion of *m*-mode controllability, the 4-mode controllability of the three-phase four-wire inverter should be discussed. Considering the symmetry of the voltage space vectors, there are three kinds of 4-mode combination, which are operating modes 1, 2, 4, and 5; operating modes 2, 3, 5, and 6; or operating modes 1, 3, 4, and 6 [1].

The matrix to analyze the 4-mode controllability of the three-phase four-wire inverter can be constructed by

$$[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \widehat{A}_3] \tag{4.1}$$

If the operating modes 1, 2, 4, and 5 are selected, $A_1^{'} = A_1$, $A_2^{'} = A_2$, $A_3^{'} = A_4$, $A_4^{'} = A_5$, $B_1^{'} = B_1$, $B_2^{'} = B_2$, $B_3^{'} = B_4$, and $B_4^{'} = B_5$, then $B' = [B_1', B_2', B_3', B_4'] = [B_1, B_2, B_4, B_5]$ is a matrix of 6×4 dimensions, $\widehat{A}_1 = [A_1\widehat{B}, A_2\widehat{B}, A_4\widehat{B}, A_5\widehat{B}]$ is of 6×16 dimensions, $\widehat{A}_2 = [A_1\widehat{A}_1, A_2\widehat{A}_1, A_4\widehat{A}_1, A_5\widehat{A}_1]$ is of 6×64 dimensions, and $\widehat{A}_3 = [A_1\widehat{A}_2, A_2\widehat{A}_2, A_4\widehat{A}_2, A_5\widehat{A}_2]$ is of 6×256 dimensions. If the operating

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modes 2, 3, 5, and 6 are selected, then $B_1^{'} = [B_1^{'}, B_2^{'}, B_3^{'}, B_4^{'}] = [B_2, B_3, B_5, B_6]$ is a matrix of 6×4 dimensions, $\widehat{A}_1 = [A_2\widehat{B}, A_3\widehat{B}, A_5\widehat{B}, A_6\widehat{B}]$ is of 6×16 dimensions, $\widehat{A}_2 = [A_2\widehat{A}_1, A_3\widehat{A}_1, A_5\widehat{A}_1, A_6\widehat{A}_1]$ is of 6×64 dimensions, and $\widehat{A}_3 = [A_2\widehat{A}_2, A_3\widehat{A}_2, A_5\widehat{A}_2, A_6\widehat{A}_2]$ is of 6×256 dimensions. If the operating modes 1, 3, 4, and 6 are selected, $B^{'} = [B_1^{'}, B_2^{'}, B_3^{'}, B_4^{'}] = [B_1, B_3, B_4, B_6]$ is a matrix of 6×4 dimensions, $\widehat{A}_1 = [A_1\widehat{B}, A_3\widehat{B}, A_4\widehat{B}, A_6\widehat{B}]$ is of 6×16 dimensions, $\widehat{A}_2 = [A_1\widehat{A}_1, A_3\widehat{A}_1, A_4\widehat{A}_1, A_6\widehat{A}_1]$ is of 6×64 dimensions, and $\widehat{A}_3 = [A_1\widehat{A}_2, A_3\widehat{A}_2, A_4\widehat{A}_2, A_6\widehat{A}_2]$ is of 6×256 dimensions.

By calculating the rank of the matrix in Eq. (4.1), the following equation is established for all three kinds of 4-mode combination.

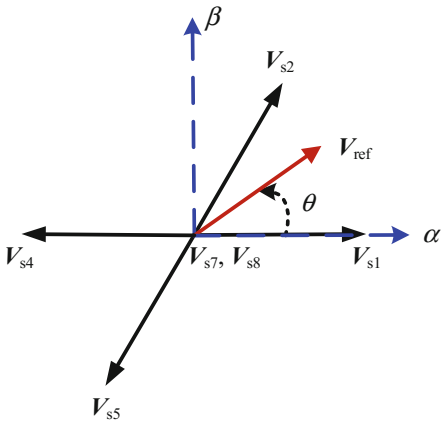
$$\begin{aligned}\operatorname{rank}[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \widehat{A}_3] = \operatorname{rank}[&B_1', \cdots, B_4', A_1'B_1', \cdots, A_1'B_4', \cdots, A_4'B_1', \cdots, A_4'B_4',\\ &A_1'^2B_1', \cdots, A_1'A_4'B_4', \cdots, A_4'A_1'B_1', \cdots, A_4'^2B_4',\\ &A_1'^3B_1', \cdots, A_1'A_4'^2B_4', \cdots, A_4'^2A_1'B_1', \cdots, A_4'^3B_4']\\ = 6 \end{aligned} \tag{4.2}$$

It can be known from Eq. (4.2) that the three-phase four-wire inverter is 4-mode controllable.

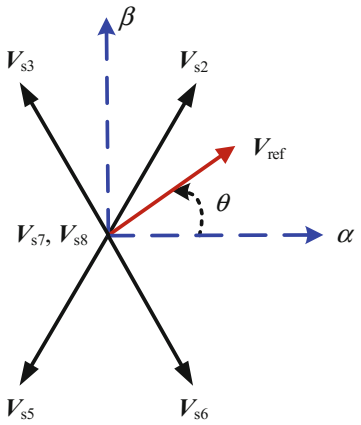
The above operating mode combination can be described by the complex plane of the voltage space vectors, which is shown in Fig. 4.1. In Fig. 4.1a, the operating modes 1, 2, 4 and 5 are represented by a complex plane of voltage vectors $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s4}$ and $\vec{V}_{s5}$; Fig. 4.1b shows the complex plane of voltage vectors $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$ and $\vec{V}_{s6}$ corresponding to the operating modes 2, 3, 5, and 6; Fig. 4.1c shows the complex planes of voltage vectors $\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$ and $\vec{V}_{s6}$ corresponding to the operating modes 1, 3, 4, and 6.

4.2 4-Mode SVPWM Strategy

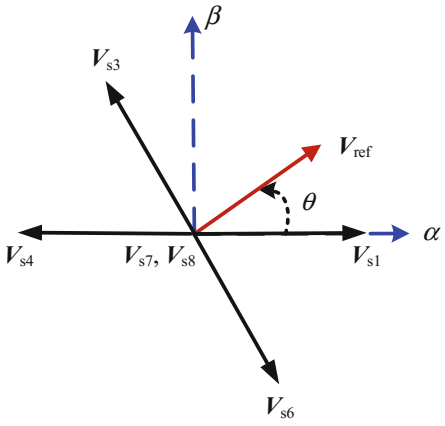
According to Theorem 2.1, the three-phase four-wire inverter is 4-mode controllable, which means that the 4-mode SVPWM can be implemented by using four basic voltage space vectors corresponding to four operating modes. The method which synthesizes the voltage space vector by using the basic voltage vectors $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s4}$ and $\vec{V}_{s5}$ corresponding to the operating modes 1, 2, 4, and 5 is named as the 4-mode SVPWM I; the one using the basic voltage vectors $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$ and $\vec{V}_{s6}$ corresponding to the operating modes 2, 3, 5, and 6 is named as the 4-mode SVPWM II; and the one using the basic voltage vectors $\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$ and $\vec{V}_{s6}$ corresponding to the operating modes 1, 3, 4, and 6 is named as the 4-mode SVPWM III.



(a) $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$.



(b) $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$.



(c) $\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s6}$.

Fig. 4.1 Distribution of 4-mode voltage space vectors

4.2.1 4-Mode SVPWM I

As shown in Fig. 4.1a, the voltage space vectors $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s4}$ and $\vec{V}_{s5}$ corresponding to the operating modes 1, 2, 4, and 5 constitute the complex plane of the 4-mode SVPWM I, in which the conventional six sectors are reduced to four sectors. The first sector is in the range of $0 \leq \theta < \frac{\pi}{3}$, corresponding to sector I of the conventional SVPWM; the second sector is in the range of $\frac{\pi}{3} \leq \theta < \pi$, corresponding to sectors II and III of the conventional SVPWM; the third sector is in the range of $\pi \leq \theta < \frac{4\pi}{3}$,

corresponding to sector IV of the conventional SVPWM; the fourth sector is in the range of $\frac{4\pi}{3} \leq \theta < 2\pi$, corresponding to sectors V and VI of the conventional SVPWM. The duration time of voltage vector in each sector can be calculated as following:

(1) If the output voltage vector of the inverter $\vec{V}_{\text{ref}}$ is located in sector I, then it is composed of $\vec{V}_{s1}$ and $\vec{V}_{s2}$, and has the following vector relationship.

$$\vec{V}_{\text{ref}} T_s = \vec{V}_{s1} T_{s1} + \vec{V}_{s2} T_{s2} \tag{4.3}$$

where T_s, T_{s1} and T_{s2} are the switching period, the duration time of $\vec{V}_{s1}$ and $\vec{V}_{s2}$, respectively.

Similar to Chap. 3, the static two-phase coordinate α-β is still used to analyze the construction process of voltage space vector in each sector. That is

$$\begin{aligned} \begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} T_s &= V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos 0 \\ \sin 0 \end{bmatrix} T_{s1} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos\frac{\pi}{3} \\ \sin\frac{\pi}{3} \end{bmatrix} T_{s2} \\ &= \frac{2}{3} V_{\text{dc}} \begin{bmatrix} 1 \\ 0 \end{bmatrix} T_{s1} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s2} \end{aligned} \tag{4.4}$$

where V_{ref} is the magnitude of $\vec{V}_{\text{ref}}$, and the magnitudes of $\vec{V}_{s1}$ and $\vec{V}_{s2}$ are $\frac{2}{3} V_{\text{dc}}$.

Taking the zero voltage vector $\vec{V}_{s7}$ into account, the duration times of $\vec{V}_{s1}$, $\vec{V}_{s2}$ and $\vec{V}_{s7}$ in one switching cycle are defined by

$$\begin{aligned} T_{s1} &= \frac{V_{\text{ref}}}{V_{\text{dc}}} \left(\frac{3}{2} \cos\theta - \frac{\sqrt{3}}{2} \sin\theta \right) T_s \\ T_{s2} &= \frac{V_{\text{ref}}}{V_{\text{dc}}} \left(\sqrt{3} \sin\theta \right) T_s \\ T_{s7} &= T_s - T_{s1} - T_{s2} \end{aligned} \tag{4.5}$$

Assuming that the synchronous modulation method is used, that is, the modulation ratio is constant. The switching sequence of two switching cycles in sector I is shown in Fig. 4.2a. It can be seen from the figure that the first cycle starts at the operating mode 1 and the output voltage vector is $\vec{V}_{s1}$. The operating mode 1 lasts for a time of T_{s1} then switches to the operating mode 7 and continues for a time of T_{s7}, then switches to the operating mode 2 and outputs $\vec{V}_{s2}$ for a time of T_{s2} till the end of the first cycle. At the beginning of the second cycle, the operating mode keeps in mode 2 and lasts for a time of T_{s2}, then switches to the operating mode 7, and finally switches to the operating mode 1 until the end of the second cycle. It is known that the upper switch VT_1 of phase a of the inverter is turned on and off twice in two

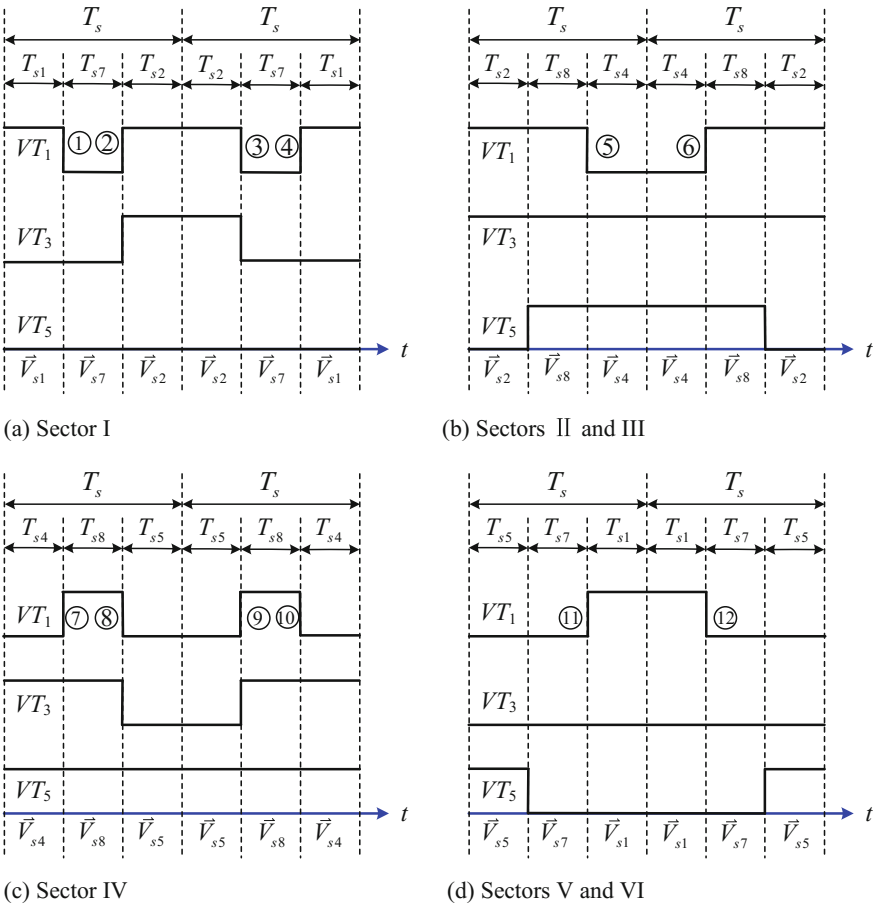


Fig. 4.2 Switching sequences of 4-mode SVPWM I

switching cycles, the upper switch VT_3 of phase b is turned on and off once, and the upper switch VT_5 of phase c remains off.

(2) If the output voltage vector $\vec{V}_{\text{ref}}$ is located in sectors II and III, then it is composed of $\vec{V}_{s2}$ and $\vec{V}_{s4}$, and the following equation is established.

$$\vec{V}_{\text{ref}} T_s = \vec{V}_{s2} T_{s2} + \vec{V}_{s4} T_{s4} \tag{4.6}$$

where T_{s4} is the duration time of $\vec{V}_{s4}$.

Thus, the relationship among T_s, T_{s2}, and T_{s4} is

$$\begin{aligned}\begin{bmatrix} V_{\text{ref}\,\alpha} \\ V_{\text{ref}\,\beta} \end{bmatrix} T_s &= V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos\frac{\pi}{3} \\ \sin\frac{\pi}{3} \end{bmatrix} T_{s2} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos\pi \\ \sin\pi \end{bmatrix} T_{s4} \\ &= \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s2} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -1 \\ 0 \end{bmatrix} T_{s4} \end{aligned} \tag{4.7}$$

where the magnitudes of $\vec{V}_{s2}$ and $\vec{V}_{s4}$ are $\frac{2}{3} V_{\text{dc}}$.

Considering the zero voltage vector $\vec{V}_{s8}$, the duration times of $\vec{V}_{s2}$, $\vec{V}_{s4}$ and $\vec{V}_{s8}$ in one switching cycle are determined by

$$\begin{aligned} T_{s2} &= \frac{V_{\text{ref}}}{V_{\text{dc}}} \left(\sqrt{3} \sin\theta \right) T_s \\ T_{s4} &= \frac{V_{\text{ref}}}{V_{\text{dc}}} \left(\frac{\sqrt{3}}{2} \sin\theta - \frac{3}{2} \cos\theta \right) T_s \\ T_{s8} &= T_s - T_{s2} - T_{s4} \end{aligned} \tag{4.8}$$

The switching sequence of two switching cycles in sectors II and III is shown in Fig. 4.2b. It can be seen from the figure that the operating mode 2 works at the beginning of the first cycle and lasts for a time of T_{s2}, then switches to the operating mode 8 and continues for a time of T_{s8}, then switches to the operating mode 4 and operates for a time of T_{s4} till the end of the first cycle. The second cycle begins with the operating mode 4, then switches to the operating mode 8, and finally switches to the operating mode 2 until the end of the cycle. Different from Fig. 4.2a, both VT_1 and VT_5 are turned on and off once in two switching cycles, while VT_3 of the phase b keeps on.

(3) If the reference voltage vector $\vec{V}_{\text{ref}}$ is located in the sector IV, then it is composed of $\vec{V}_{s4}$ and $\vec{V}_{s5}$, that is

$$\vec{V}_{\text{ref}} T_s = \vec{V}_{s4} T_{s4} + \vec{V}_{s5} T_{s5} \tag{4.9}$$

where T_{s5} is the duration time of $\vec{V}_{s5}$.

Thus, the relationship among T_s, T_{s4} and T_{s5} is established as following:

$$\begin{aligned}\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\,\beta} \end{bmatrix} T_s &= V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos\pi \\ \sin\pi \end{bmatrix} T_{s4} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \cos\frac{4\pi}{3} \\ \sin\frac{4\pi}{3} \end{bmatrix} T_{s5} \\ &= \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -1 \\ 0 \end{bmatrix} T_{s4} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s5} \end{aligned} \tag{4.10}$$

Considering the zero voltage vector $\vec{V}_{s8}$, the duration times of $\vec{V}_{s4}$, $\vec{V}_{s5}$, and $\vec{V}_{s8}$ in one switching cycle are expressed by

$$\begin{aligned} T_{s4} &= \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{\sqrt{3}}{2}\sin\theta - \frac{3}{2}\cos\theta\right)T_s \\ T_{s5} &= -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\sqrt{3}\sin\theta\right)T_s \\ T_{s8} &= T_s - T_{s4} - T_{s5} \end{aligned} \tag{4.11}$$

The switching sequence of two switching cycles in sector IV is shown in Fig. 4.2c. Similar to the above analysis, it is found that in two switching cycles, VT_1 is turned on and off twice, VT_3 is turned on and off once, but VT_5 keeps on.

(4) If the reference voltage vector $\vec{V}_{\text{ref}}$ is located in sectors V and VI, then it is composed of $\vec{V}_{s5}$ and $\vec{V}_{s1}$, that is

$$\vec{V}_{\text{ref}}T_s = \vec{V}_{s5}T_{s5} + \vec{V}_{s1}T_{s1} \tag{4.12}$$

Thus, the relationship among T_s, T_{s5}, and T_{s1} is expressed by

$$\begin{aligned} \begin{bmatrix} V_{\text{ref}\,\alpha} \\ V_{\text{ref}\,\beta} \end{bmatrix} T_s &= V_{\text{ref}}\begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3}V_{\text{dc}}\begin{bmatrix} \cos\frac{4\pi}{3} \\ \sin\frac{4\pi}{3} \end{bmatrix} T_{s5} + \frac{2}{3}V_{\text{dc}}\begin{bmatrix} \cos 2\pi \\ \sin 2\pi \end{bmatrix} T_{s1} \\ &= \frac{2}{3}V_{\text{dc}}\begin{bmatrix} -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s5} + \frac{2}{3}V_{\text{dc}}\begin{bmatrix} 1 \\ 0 \end{bmatrix} T_{s1} \end{aligned} \tag{4.13}$$

Considering the zero voltage vector $\vec{V}_{s7}$, the duration times of $\vec{V}_{s5}$, $\vec{V}_{s1}$, and $\vec{V}_{s7}$ in one switching cycle are determined by

$$\begin{aligned} T_{s5} &= -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\sqrt{3}\sin\theta\right)T_s \\ T_{s1} &= \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta - \frac{\sqrt{3}}{2}\sin\theta\right)T_s \\ T_{s7} &= T_s - T_{s5} - T_{s1} \end{aligned} \tag{4.14}$$

The switching sequence of two switching cycles in sectors V and VI is shown in Fig. 4.2d. Similar to Fig. 4.2b, both VT_1 and VT_5 are turned on and off once in two switching cycles, but VT_3 remains off.

4.2.2 4-*Mode SVPWM II*

As shown in Fig. 4.1b, the 4-mode SVPWM II consists of the voltage space vector $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$, and $\vec{V}_{s6}$, which corresponding to the operating modes 2, 3, 5, and 6, respectively. Thus, six sectors of the conventional SVPWM are reduced to four sectors in the 4-mode SVPWM II, where the first sector is located in the range of $-\frac{\pi}{3} \leq \theta < \frac{\pi}{3}$, corresponding to sectors VI and I of the conventional SVPWM; the second sector is located in the range of $\frac{\pi}{3} \leq \theta < \frac{2\pi}{3}$, corresponding to sector II of the conventional SVPWM; the third sector is located in the range of $\frac{2\pi}{3} \leq \theta < \frac{4\pi}{3}$, corresponding to sectors III and IV of the conventional SVPWM; the fourth sector is located in the range of $\frac{4\pi}{3} \leq \theta < \frac{5\pi}{3}$, corresponding to sector V of the conventional SVPWM.

Similarly, the calculation of duration time for the voltage space vector in each sector can be carried out by referring to the calculation method of the 4-mode SVPWM I.

If the output voltage vector $\vec{V}_{\text{ref}}$ is located in sectors VI and I, then it is composed of $\vec{V}_{s2}$ and $\vec{V}_{s6}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s6} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s2} \tag{4.15}$$

If $\vec{V}_{\text{ref}}$ is located in sector II, then it is composed of $\vec{V}_{s2}$ and $\vec{V}_{s3}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s2} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s3} \tag{4.16}$$

If $\vec{V}_{\text{ref}}$ is located in sectors III and IV, then it is composed of $\vec{V}_{s3}$ and $\vec{V}_{s5}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s3} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s5} \tag{4.17}$$

If $\vec{V}_{\text{ref}}$ is located in sector V, then it is composed of $\vec{V}_{s5}$ and $\vec{V}_{s6}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s6} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s5} \tag{4.18}$$

Table 4.1 Voltage space vector and its duration time of 4-mode SVPWM II

Sector	Voltage space vector	Duration time
VI, I $\left(-\frac{\pi}{3} \le \theta < \frac{\pi}{3}\right)$	$\vec{V}_{s6}, \vec{V}_{s2}$	$T_{s6} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta - \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s2} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s8} = T_s - T_{s6} - T_{s2}$
II $\left(\frac{\pi}{3} \le \theta < \frac{2\pi}{3}\right)$	$\vec{V}_{s2}, \vec{V}_{s3}$	$T_{s2} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{\sqrt{3}}{2}\sin\theta + \frac{3}{2}\cos\theta\right)T_s$ $T_{s3} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{\sqrt{3}}{2}\sin\theta - \frac{3}{2}\cos\theta\right)T_s$ $T_{s8} = T_s - T_{s2} - T_{s3}$
III, IV $\left(\frac{2\pi}{3} \le \theta < \frac{4\pi}{3}\right)$	$\vec{V}_{s3}, \vec{V}_{s5}$	$T_{s3} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{\sqrt{3}}{2}\sin\theta - \frac{3}{2}\cos\theta\right)T_s$ $T_{s5} = -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{\sqrt{3}}{2}\sin\theta + \frac{3}{2}\cos\theta\right)T_s$ $T_{s7} = T_s - T_{s3} - T_{s5}$
V $\left(\frac{4\pi}{3} \le \theta < \frac{5\pi}{3}\right)$	$\vec{V}_{s5}, \vec{V}_{s6}$	$T_{s5} = -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s6} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta - \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s7} = T_s - T_{s5} - T_{s6}$

According to Eqs. (4.15–4.18), the duration time of the voltage space vector in each sector can be calculated and listed in Table 4.1, and the corresponding switching sequence of operating modes in each sector is shown in Fig. 4.3.

4.2.3 4-Mode SVPWM III

As shown in Fig. 4.1c, the 4-mode SVPWM III consists of the voltage vectors $\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, and $\vec{V}_{s6}$ corresponding to the operating modes 1, 3, 4, and 6, respectively. There are four sectors of the 4-mode SVPWM III: the first one is in the range of $-\frac{\pi}{3} \le \theta < 0$, corresponding to sector VI of the conventional SVPWM; the second one is in the range of $0 \le \theta < \frac{2\pi}{3}$, corresponding to sectors II and I of the conventional SVPWM; the third one is in the range of $\frac{2\pi}{3} \le \theta < \pi$, corresponding to

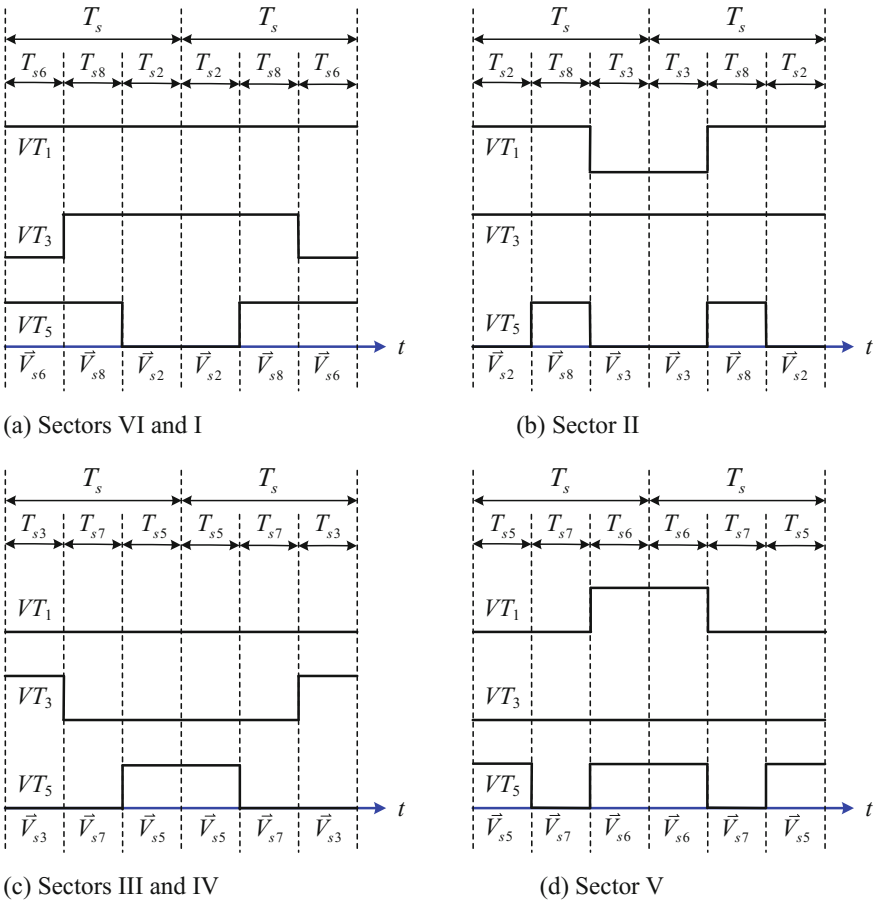


Fig. 4.3 Switching sequences of 4-mode SVPWM II

sector III of the conventional SVPWM; the fourth one is in the range of $\pi \leq \theta < \frac{5\pi}{3}$, corresponding to sectors IV and V of the conventional SVPWM.

If $\vec{V}_{\text{ref}}$ is located in sector VI, then it is composed of $\vec{V}_{s6}$, $\vec{V}_{s1}$, and $\vec{V}_{s7}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\alpha} \\ V_{\text{ref}\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s6} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} 1 \\ 0 \end{bmatrix} T_{s1} \tag{4.19}$$

If $\vec{V}_{\text{ref}}$ is located in sectors I and II, then it is composed of $\vec{V}_{s1}$, $\vec{V}_{s3}$, and $\vec{V}_{s7}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\,\alpha} \\ V_{\text{ref}\,\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} 1 \\ 0 \end{bmatrix} T_{s1} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s3} \tag{4.20}$$

If $\vec{V}_{\text{ref}}$ is located in sector III, then it is composed of $\vec{V}_{s3}$, $\vec{V}_{s4}$, and $\vec{V}_{s8}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\,\alpha} \\ V_{\text{ref}\,\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -\frac{1}{2} \\ \frac{\sqrt{3}}{2} \end{bmatrix} T_{s3} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -1 \\ 0 \end{bmatrix} T_{s4} \tag{4.21}$$

If $\vec{V}_{\text{ref}}$ is located in sectors IV and V, then it is composed of $\vec{V}_{s4}$, $\vec{V}_{s6}$, and $\vec{V}_{s8}$, and the following relationship is built:

$$\begin{bmatrix} V_{\text{ref}\,\alpha} \\ V_{\text{ref}\,\beta} \end{bmatrix} T_s = V_{\text{ref}} \begin{bmatrix} \cos\theta \\ \sin\theta \end{bmatrix} T_s = \frac{2}{3} V_{\text{dc}} \begin{bmatrix} -1 \\ 0 \end{bmatrix} T_{s4} + \frac{2}{3} V_{\text{dc}} \begin{bmatrix} \frac{1}{2} \\ -\frac{\sqrt{3}}{2} \end{bmatrix} T_{s6} \tag{4.22}$$

According to Eqs. (4.19–4.22), the duration time of the voltage space vector in each sector can be calculated and summarized in Table 4.2, and the corresponding switching sequence of operating modes in each sector is shown in Fig. 4.3.

4.3 Characteristic Analysis

4.3.1 Switching Times and Switching Frequency

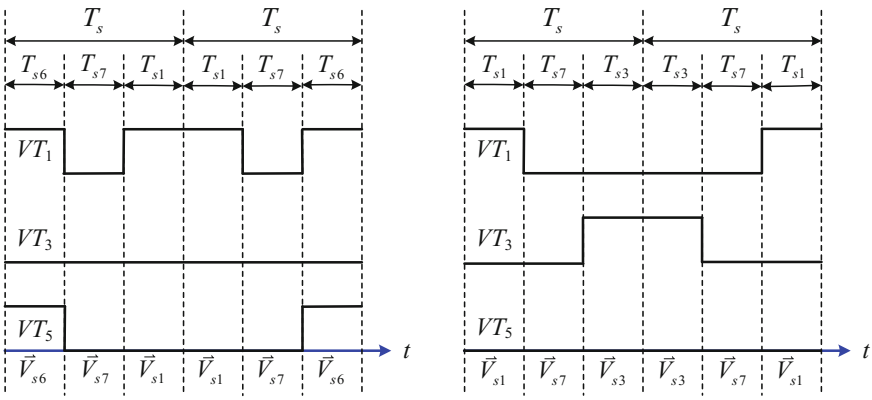
According to the switching strategies of the 4-mode SVPWM I, II, III shown in Figs. 4.2, 4.3, and 4.4, the switching sequences within one cycle of output voltage are summarized in Tables 4.3, 4.4, and 4.5, respectively. Compared with the conventional SVPWM, the number of switching times of the 4-mode SVPWM is reduced by 11/18. Therefore, the equivalent switching frequency of the 4-mode SVPWM is only 7/18 of that of the conventional SVPWM.

4.3.2 Output Voltage

The simulation parameters of the three-phase four-wire inverter are set as follows: three-phase output filter with inductor $L = 4$ mH and capacitor $C = 6.8$ μF, the equivalent line resistor $r = 0.5\ \Omega$, the carrier frequency is 10 kHz, and the fundamental frequency of the output voltage is 50 Hz. The simulation waveform of the output line voltages is shown in Fig. 4.5, which are all sinusoidal.

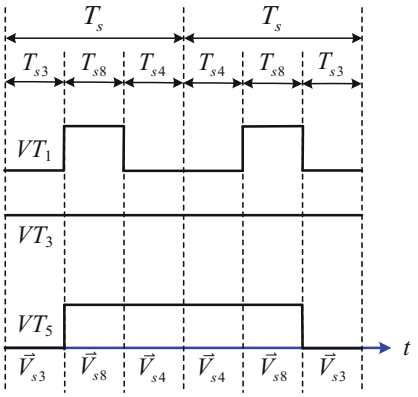
Table 4.2 Space vector and its duration time of 4-mode SVPWM III

Sector	Voltage space vector	Duration time
VI $\left(-\frac{\pi}{3} \le \theta < 0\right)$	$\vec{V}_{s6}, \vec{V}_{s1}$	$T_{s6} = -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\sqrt{3}\sin\theta\right)T_s$ $T_{s1} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s7} = T_s - T_{s6} - T_{s1}$
I, II $0 \le \theta < \frac{2\pi}{3}$	$\vec{V}_{s1}, \vec{V}_{s3}$	$T_{s1} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s3} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\sqrt{3}\sin\theta\right)T_s$ $T_{s7} = T_s - T_{s1} - T_{s3}$
III $\left(\frac{2\pi}{3} \le \theta < \pi\right)$	$\vec{V}_{s3}, \vec{V}_{s4}$	$T_{s3} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\sqrt{3}\sin\theta\right)T_s$ $T_{s4} = -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s8} = T_s - T_{s3} - T_{s4}$
IV, V $\left(\pi \le \theta < \frac{5\pi}{3}\right)$	$\vec{V}_{s4}, \vec{V}_{s6}$	$T_{s4} = -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\frac{3}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta\right)T_s$ $T_{s6} = -\frac{V_{\text{ref}}}{V_{\text{dc}}}\left(\sqrt{3}\sin\theta\right)T_s$ $T_{s8} = T_s - T_{s1} - T_{s3}$

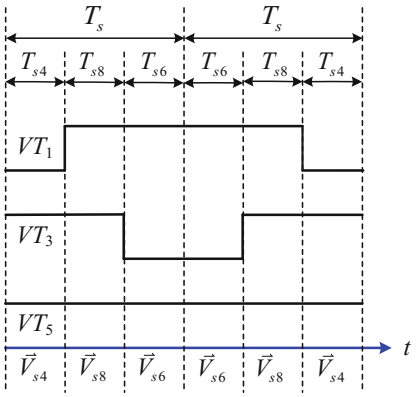


(a) Sector VI (b) Sectors I and II

Fig. 4.4 Switching sequences of 4-mode SVPWM III



(c) Sector III



(d) Sectors IV and V

Fig. 4.4 (continued)

Table 4.3 Switching sequences of conventional SVPWM and 4-mode SVPWM I

Sector	Conventional SVPWM	Switching times	4-mode SVPWM I	Switching times
I	000-100-110-111-110-100-000-100-110-111-110-100-000	12	100-000-110-000-100	6
II	000-010-110-111-110-010-000-010-110-111-110-010-000	12	110-111-011-111-110	4
III	000-010-011-111-011-010-000-010-011-111-011-010-000	12	110-111-011-111-110	4
IV	000-001-011-111-011-001-000-001-011-111-011-001-000	12	011-111-001-111-011	6
V	000-001-101-111-101-001-000-001-101-111-101-001-000	12	001-000-100-000-001	4
VI	000-100-101-111-101-100-000-100-101-111-101-100-000	12	001-000-100-000-001	4
Total		72		28

Table 4.4 Switching sequences of conventional SVPWM and 4-mode SVPWM II

Sector	Conventional SVPWM	Switching times	4-mode SVPWM II	Switching times
I	000-100-110-111-110-100-000-100-110-111-110-100-000	12	101-111-110-111-101	4
II	000-010-110-111-110-010-000-010-110-111-110-010-000	12	110-111-010-111-110	6
III	000-010-011-111-011-010-000-010-011-111-011-010-000	12	010-000-001-000-010	4
IV	000-001-011-111-011-001-000-001-011-111-011-001-000	12	010-000-001-000-010	4
V	000-001-101-111-101-001-000-001-101-111-101-001-000	12	001-000-101-000-001	6
VI	000-100-101-111-101-100-000-100-101-111-101-100-000	12	101-111-110-111-101	4
Total		72		28

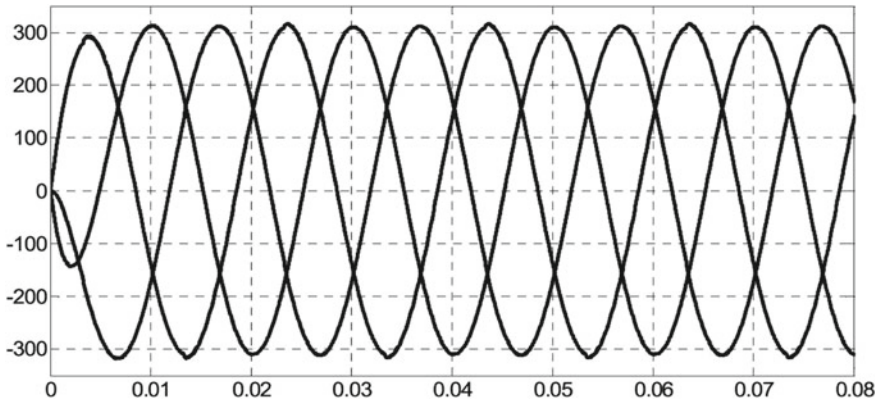


Fig. 4.5 Output line voltages of 4-mode SVPWM

Table 4.5 Switching sequences of conventional SVPWM and 4-mode SVPWM III

Sector	Conventional SVPWM	Switching times	4-mode SVPWM III	Switching times
I	000-100-110-111-110-100-000-100-110-111-110-100-000	12	100-000-010-000-100	4
II	000-010-110-111-110-010-000-010-110-111-110-010-000	12	100-000-010-000-100	4
III	000-010-011-111-011-010-000-010-011-111-011-010-000	12	010-111-011-111-010	6
IV	000-001-011-111-011-001-000-001-011-111-011-001-000	12	001-111-101-111-001	4
V	000-001-101-111-101-001-000-001-101-111-101-001-000	12	011-111-101-111-011	4
VI	000-100-101-111-101-100-000-100-101-111-101-100-000	12	101-000-100-000-101	6
Total		72		28

4.3.3 Comparison with 3-Mode SVPWM

Comparing the 3-mode SVPWM and the 4-mode SVPWM, it is found that both of them can reduce the amount of calculation, switching times, and equivalent switching frequency by reducing the sectors of the conventional SVPWM. The difference is that each sector in the 3-mode SVPWM has the same size interval, while the 4-mode SVPWM has different sector size, resulting in different switching times per sector. The comparison of switching sequences between the 3-mode SVPWM I and the 4-mode SVPWM I is listed in Table 4.6.

4.4 Geometric Meaning of *m*-Mode SVPWM

Referring to the voltage space vector distribution of the three-phase four-wire inverter in Fig. 3.3, a synthesized vector $\vec{V}_{\text{ref}}$ can be constructed by using the symmetrical

Table 4.6 Comparison between 3-mode SVPWM I and 4-mode SVPWM I

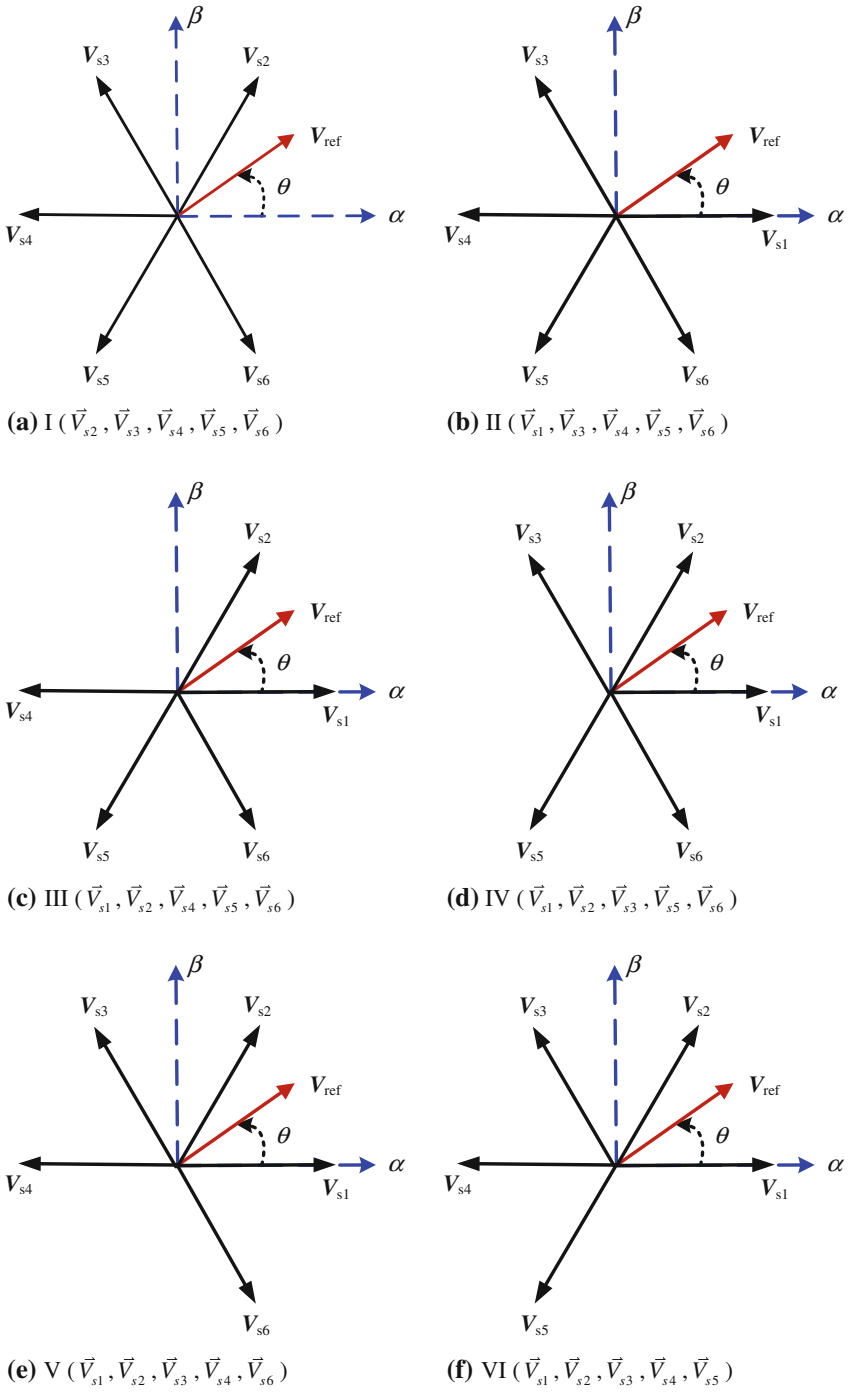
Sector	3-mode SVPWM I	Switching times	4-mode SVPWM I	Switching times
I	100-000-010-000-100	4	100-000-110-000-100	6
II	100-000-010-000-100	4	110-111-011-111-110	4
III	010-000-001-000-010	4	110-111-011-111-110	4
IV	010-000-001-000-010	4	011-111-001-111-011	6
V	001-000-100-000-001	4	001-000-100-000-001	4
VI	001-000-100-000-001	4	001-000-100-000-001	4
Total		24		28

basic voltage space vectors shown in Figs. 3.4, 3.7, and 4.1, or using the asymmetric basic space vectors as long as the angle range of every sector is less than π. Therefore, for the 3-mode SVPWM, only two construction methods shown in Figs. 3.4 and 3.7 are available; for the 4-mode SVPWM, only three construction methods shown in Fig. 4.1 are available; but for the 5-mode SVPWM, there will be six construction methods, which are shown in Fig. 4.6.

In addition, according to the construction method of the 3-mode SVPWM III, new hybrid *m*-mode SVPWMs can be formed based on the 4-mode and 5-mode SVPWMs, to further improve the performance of application.

4.5 Summary

This chapter further studies the control strategy of the 4-mode SVPWM for the three-phase four-wire inverter. The 4-mode SVPWM reduces the number of sectors of conventional SVPWM from six to four, which reduces the switching times of switches by 11/18, that is, the equivalent switching frequency is reduced to 7/18 of that of the conventional SVPWM. Similar to the 3-mode SVPWM, the purpose of reducing the calculation amount, the number of switching times, and the switching frequency is achieved. Considering the constraint that the geometric angle of each sector cannot be larger than π, there are only two basic construction methods for the 3-mode SVPWM, only three for the 4-mode SVPWM and consequently 6 for the 5-mode SVPWM. In order to improve the control characteristics of *m*-mode SVPWM, the hybrid *m*-mode SVPWM method can be used for 4-mode and 5-mode SVPWMs as needed.



(a) I ($\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$)

(b) II ($\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$)

(c) III ($\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$)

(d) IV ($\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$)

(e) V ($\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s6}$)

(f) VI ($\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$)

Fig. 4.6 Space vector construction method of 5-mode SVPWMs

Reference

1. Li X, Zhang B, Qiu D (2015) Three-mode pulse-width modulation of a three-phase four-wire inverter. IET Power Electron 8(8):1483–1489

Chapter 5
6-Mode SVPWM for Nine-Switch Dual-Output Inverter

Manufacturing industries such as textiles, paper, and steel require high-performance control of multiple variable-frequency motors simultaneously. Normally, one motor is controlled by one inverter. However, with the continuous improvement of the cost performance requirements of the variable-frequency system, driving multiple motors by only one inverter has become a development trend, thus the nine-switch inverter with two outputs was proposed. In this chapter, the *m*-mode SVPWM method is applied to the nine-switch dual-output inverter, which not only verifies and expands the application of *m*-mode SVPWM, but also puts forward a novel SVPWM technique different from the existing ones to further enhance the performance of inverters.

5.1 Operating Principle of Nine-Switch Dual-Output Inverter

The nine-switch inverter shown in Fig. 5.1 is a three-phase dual-output inverter in fact [1]. There are three switching devices in each leg, and the middle switches VT_4, VT_5, and VT_6 are shared by the upper and lower sub-inverters. Therefore, the upper sub-inverter is composed of VT_1, VT_2, VT_3, VT_4, VT_5, and VT_6, while the lower one is composed of VT_4, VT_5, VT_6, VT_7, VT_8, and VT_9.

According to the ON/OFF state of the switches, there are 14 operating modes for the nine-switch dual-output inverter, which can be represented by 14 basic voltage space vectors, $\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$, $\vec{V}_{s7}$, $\vec{V}_{s8}$, $\vec{V}_{s9}$, $\vec{V}_{s10}$, $\vec{V}_{s11}$, $\vec{V}_{s12}$, $\vec{V}_{s13}$, $\vec{V}_{s14}$, respectively. In order to simplify the representation of each operating mode, the ON/OFF state of the upper switches of the upper/lower sub-inverter is used, where "1" means "ON" and "0" means "OFF". Letter "*u*" or "*l*" is put before the binary combination to distinguish the upper and lower inverters, where "*u*" denotes the upper sub-inverter and "*l*" denotes the lower sub-inverter. According to Fig. 5.2, the operating modes and their corresponding switching states are summarized in Table 5.1.

B. Zhang and D. Qiu, *m-Mode SVPWM Technique for Power Converters*, CPSS Power Electronics Series, https://doi.org/10.1007/978-981-13-1382-0_5

Table 5.1 Operating modes of the nine-switch dual-output inverter

Mode	VT_1	VT_2	VT_3	VT_4	VT_5	VT_6	VT_7	VT_8	VT_9	Voltage vector	Binary representation
1	ON	OFF	OFF	OFF	ON	ON	ON	ON	ON	$\vec{V}_{s1}$	$u100$
2	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	$\vec{V}_{s2}$	$u110$
3	OFF	ON	OFF	ON	OFF	ON	ON	ON	ON	$\vec{V}_{s3}$	$u010$
4	OFF	ON	ON	ON	OFF	OFF	ON	ON	ON	$\vec{V}_{s4}$	$u011$
5	OFF	OFF	ON	ON	ON	OFF	ON	ON	ON	$\vec{V}_{s5}$	$u001$
6	ON	OFF	ON	OFF	ON	OFF	ON	ON	ON	$\vec{V}_{s6}$	$u101$
7	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	$\vec{V}_{s7}$	$l100$
8	ON	ON	ON	ON	ON	OFF	OFF	OFF	ON	$\vec{V}_{s8}$	$l110$
9	ON	ON	ON	OFF	ON	OFF	ON	OFF	ON	$\vec{V}_{s9}$	$l010$
10	ON	ON	ON	OFF	ON	ON	ON	OFF	OFF	$\vec{V}_{s10}$	$l011$
11	ON	ON	ON	OFF	OFF	ON	ON	ON	OFF	$\vec{V}_{s11}$	$l001$
12	ON	ON	ON	ON	OFF	ON	OFF	ON	OFF	$\vec{V}_{s12}$	$l101$
13	ON	ON	ON	OFF	OFF	OFF	ON	ON	ON	$\vec{V}_{s13}$	111
14	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	$\vec{V}_{s14}$	000

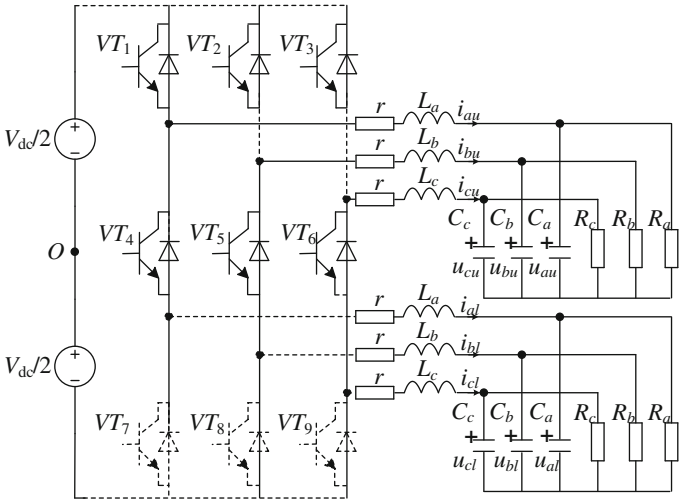


Fig. 5.1 Nine-switch dual-output inverter

As $\vec{V}_{s13}$ and $\vec{V}_{s14}$ are the zero voltage space vectors, the distribution of other 12 non-zero voltage space vectors on the complex plane is shown in Fig. 5.3. It is found that the complex plane is symmetrically divided into six sectors (I–VI), and the voltage vectors of upper sub-inverter ($\vec{V}_{s1}$, $\vec{V}_{s2}$, $\vec{V}_{s3}$, $\vec{V}_{s4}$, $\vec{V}_{s5}$, $\vec{V}_{s6}$) completely coincide with those of the lower sub-inverter ($\vec{V}_{s7}$, $\vec{V}_{s8}$, $\vec{V}_{s9}$, $\vec{V}_{s10}$, $\vec{V}_{s11}$, $\vec{V}_{s12}$).

Since the nine-switch dual-output inverter can be considered as a combination of two three-phase inverters from the topological aspect, the conventional SVPWM or SPWM strategies can be used to modulate the nine-switch dual-output inverter [2–4]. Table 5.2 lists the switching sequence of the conventional SVPWM for the nine-switch dual-output inverter. It can be seen that four basic voltage space vectors are used to form the reference output voltage vector in each sector, in which two basic vectors compose the output voltage vector of the upper sub-inverter and the other two compose that of the lower sub-inverter.

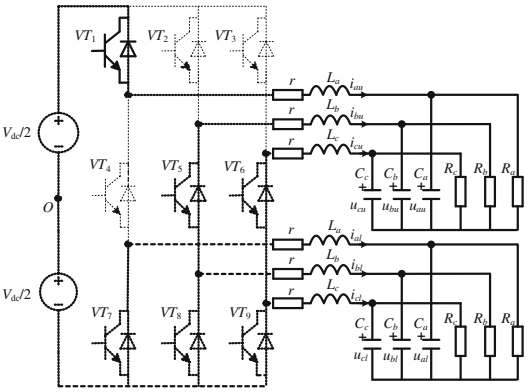
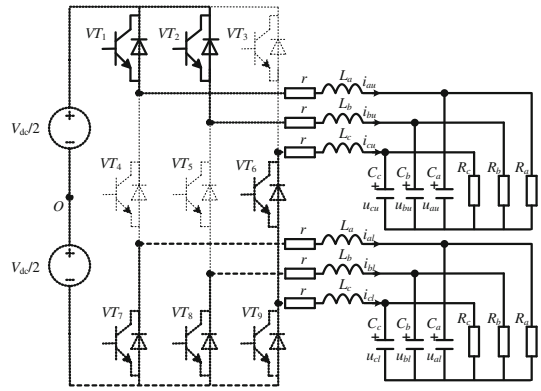
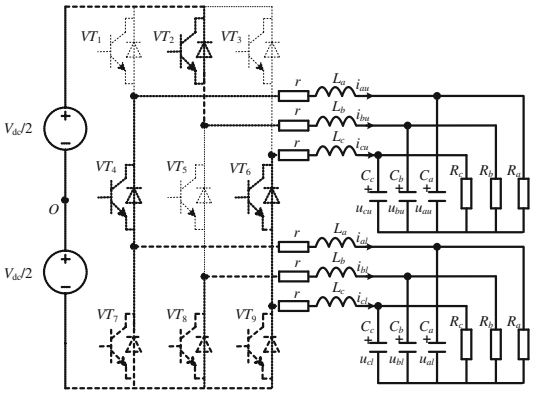


Fig. 5.2 Equivalent circuits of the nine-switch dual-output inverter

(a) Operating mode 1

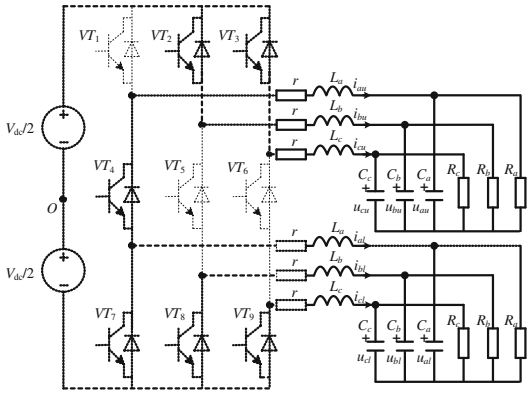


(b) Operating mode 2

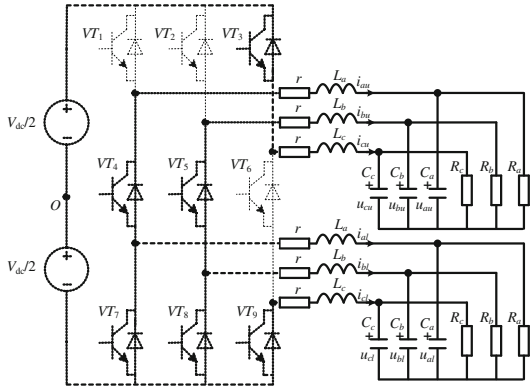


(c) Operating mode 3

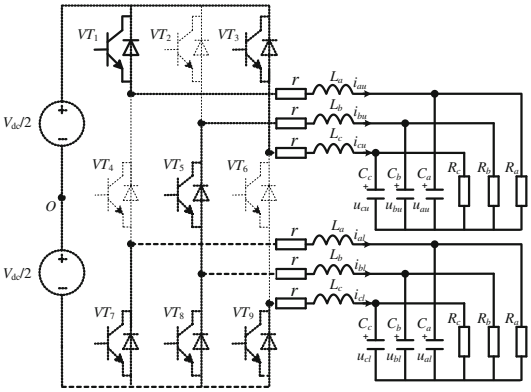
Fig. 5.2 (continued)



(d) Operating mode 4

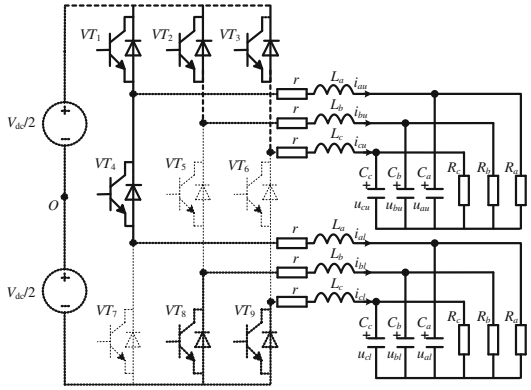


(e) Operating mode 5

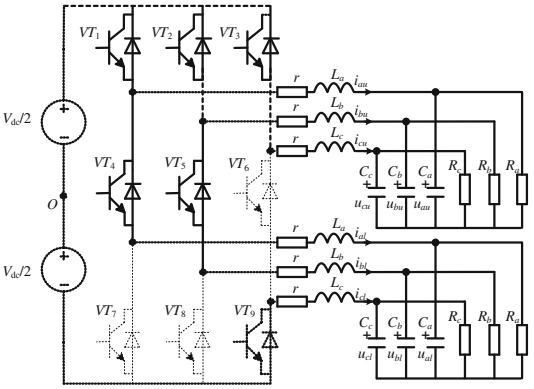


(f) Operating mode 6

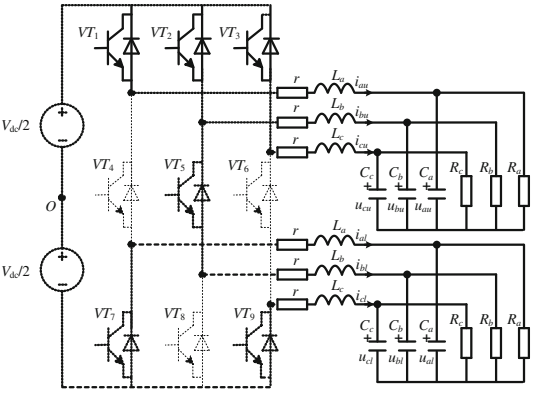
Fig. 5.2 (continued)



(g) Operating mode 7

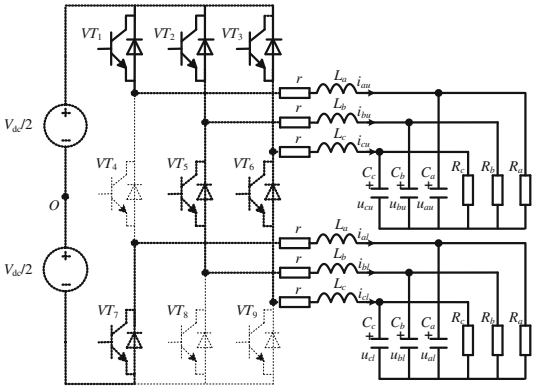


(h) Operating mode 8

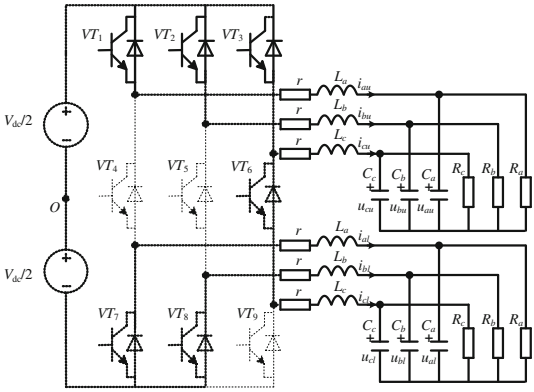


(i) Operating mode 9

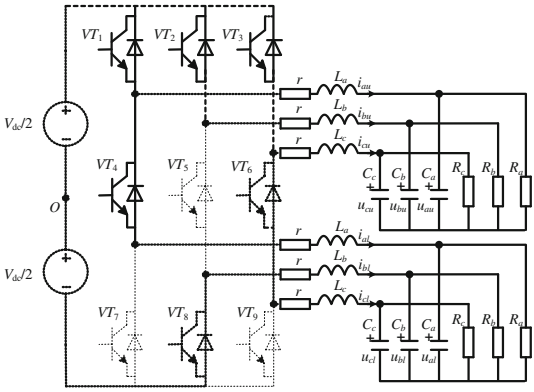
Fig. 5.2 (continued)



(j) Operating mode 10

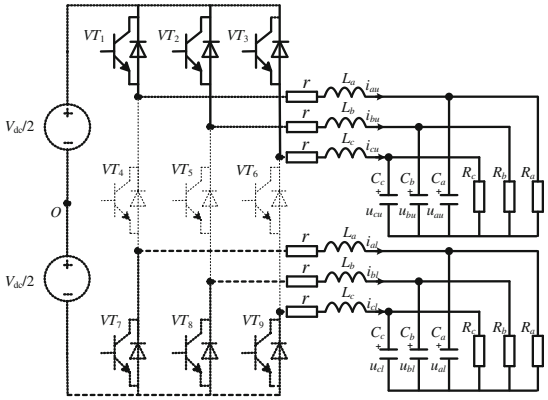


(k) Operating mode 11

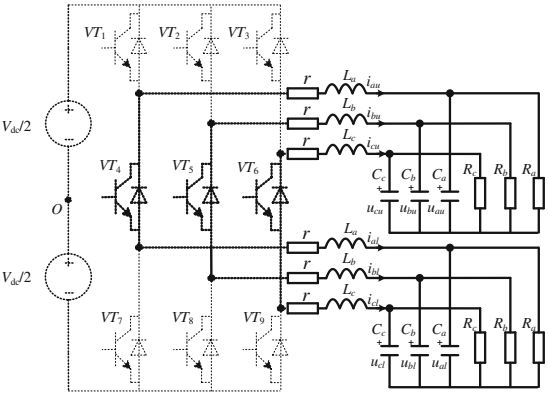


(l) Operating mode 12

Fig. 5.2 (continued)



(m) Operating mode 13



(n) Operating mode 14

Fig. 5.3 Distribution of basic voltage space vectors

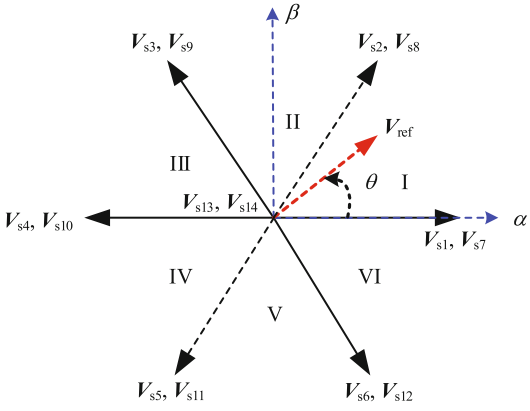


Table 5.2 Switching sequences of conventional SVPWM

Sector	Switching sequence	Switching times
I	000-*u*100-*u*110-111-*u*110-*u*100-000-*l*100-*l*110-111-*l*110-*l*100-000	12
II	000-*u*010-*u*110-111-*u*110-*u*010-000-*l*010-*l*110-111-*l*110-*l*010-000	12
III	000-*u*010-*u*011-111-*u*011-*u*010-000-*l*010-*l*011-111-*l*011-*l*010-000	12
IV	000-*u*001-*u*011-111-*u*011-*u*001-000-*l*001-*l* 011-111-*l*011-*l*001-000	12
V	000-*u*001-*u*101-111-*u*101-*u*001-000-*l*001-*l*101-111-*l*101-*l*001-000	12
VI	000-*u*100-*u*101-111-*u*101-*u*100-000-*l*100-*l*101-111-l101-*l*100-000	12
Total		72

5.2 6-Mode SVPWM Strategy

5.2.1 Switched Linear System Model

The state variable of the nine-switch inverter is represented by $x = \left[x_u\ x_l\right]^{\mathrm{T}}$, where x_u is the state variable matrix of the upper sub-inverter, and x_l is that of the lower sub-inverter. If the output inductor currents and the capacitor voltages of two loads are selected, then $x_u = [i_{au},\ i_{bu},\ i_{cu},\ u_{au},\ u_{bu},\ u_{cu}]^{\mathrm{T}}$ and $x_l = [i_{al},\ i_{bl},\ i_{cl},\ u_{al},\ u_{bl},\ u_{cl}]^{\mathrm{T}}$. According to Fig. 3.1, it is assumed that the values of all capacitors, all inductors, and all resistors are equal, that is, $C_a = C_b = C_c = C$, $L_a = L_b = L_c = L$, $R_a = R_b = R_c = R$. Then the switched linear system model of the nine-switch dual-output inverter similar to Eq. (2.1) can be established, where

$$A_1 = \cdots = A_{14} = \begin{bmatrix} A_{a1} & 0 \\ 0 & \mathrm{A_{a2}} \end{bmatrix} \tag{5.1}$$

$$\left[B_1\ B_2\ \cdots\ B_{14}\right] = \begin{bmatrix} B_{a1} & 0 \\ 0 & B_{a2} \end{bmatrix} \tag{5.2}$$

$$C_1 = \cdots = C_{14} = \begin{bmatrix} C_{a1} & 0 \\ 0 & C_{a2} \end{bmatrix} \tag{5.3}$$

$$A_{a1} = A_{a2} = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} \end{bmatrix} \tag{5.4}$$

$$B_{a1} = B_{a2} = \begin{bmatrix} \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} \\ -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} \\ -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5.5}$$

$$C_{a1} = \begin{bmatrix} 0\,0\,0\,1\,0\,0\,0\,0\,0\,0\,0\,0 \\ 0\,0\,0\,0\,1\,0\,0\,0\,0\,0\,0\,0 \\ 0\,0\,0\,0\,0\,1\,0\,0\,0\,0\,0\,0 \end{bmatrix} \tag{5.6}$$

$$C_{a2} = \begin{bmatrix} 0\,0\,0\,0\,0\,0\,0\,0\,0\,1\,0\,0 \\ 0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,1\,0 \\ 0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,1 \end{bmatrix} \tag{5.7}$$

Since the control between the upper and lower sub-inverters of the nine-switch dual-output inverter is coupled, the switching sequence can be expressed as

$$\sigma = \psi\left(i_{au}, i_{cu}, i_{au}, u_{au}, u_{bu}, u_{cu}, i_{al}, i_{cl}, i_{al}, u_{al}, u_{bl}, u_{cl}, \sigma^{-}, \theta\right), \tag{5.8}$$

where $\sigma \in (1, 2, \ldots, 14)$. The upper and lower sub-inverters should meet the switching constraints listed in Table 5.3.

Table 5.3 Switching constraints of upper and lower sub-inverters

σ	1, 7	2, 8	3, 9	4, 10	5, 11	6, 12
u_{au}, u_{al}	$u_{au}, u_{al} > 0$	$u_{au}, u_{al} > 0$	$u_{au}, u_{al} < 0$	$u_{au}, u_{al} < 0$	$u_{au}, u_{al} < 0$	$u_{au}, u_{al} > 0$
u_{bu}, u_{bl}	$u_{bu}, u_{bl} < 0$	$u_{bu}, u_{bl} > 0$	$u_{bu}, u_{bl} > 0$	$u_{bu}, u_{bl} > 0$	$u_{bu}, u_{bl} < 0$	$u_{bu}, u_{bl} < 0$
u_{cu}, u_{cl}	$u_{cu}, u_{cl} < 0$	$u_{cu}, u_{cl} < 0$	$u_{cu}, u_{cl} < 0$	$u_{cu}, u_{cl} > 0$	$u_{cu}, u_{cl} > 0$	$u_{cu}, u_{cl} > 0$
θ	$-\frac{\pi}{3} < \theta \leq \frac{\pi}{3}$	$0 < \theta \leq \frac{2\pi}{3}$	$\frac{\pi}{3} < \theta \leq \pi$	$\frac{2\pi}{3} < \theta \leq \frac{4\pi}{3}$	$\pi < \theta \leq \frac{5\pi}{3}$	$\frac{4\pi}{3} < \theta \leq 2\pi$
σ^{-}	2, 6, 8, 12	1, 3, 7, 9	2, 4, 8, 10	3, 5, 9, 11	4, 6, 10, 12	1, 5, 7, 11

5.2.2 m-*Mode Controllability*

Corresponding to Eq. (2.6), the matrix to analyze the state controllability of nine-switch dual-output inverter can be constructed as follows.

$$\left[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \widehat{A}_3, \widehat{A}_4, \widehat{A}_5, \widehat{A}_6, \widehat{A}_7, \widehat{A}_8, \widehat{A}_9, \widehat{A}_{10}, \widehat{A}_{11}\right], \tag{5.9}$$

where $\widehat{B} = [B_1, B_2, \ldots, B_{12}]$ is a matrix of 12×12 dimensions; $\widehat{A}_1 = \left[A_1\widehat{B}, A_2\widehat{B}, \ldots, A_{12}\widehat{B}\right]$ is of 12×12^2 dimensions; $\widehat{A}_2 = \left[A_1\widehat{A}_1, A_2\widehat{A}_1, \ldots, A_{12}\widehat{A}_1\right]$ is of 12×12^3 dimensions; $\widehat{A}_3 = \left[A_1\widehat{A}_2, A_2\widehat{A}_2, \ldots, A_{12}\widehat{A}_2\right]$ is of 12×12^4 dimensions; …; $\widehat{A}_{11} = \left[A_1\widehat{A}_{10}, A_2\widehat{A}_{10}, \ldots, A_{12}\widehat{A}_{10}\right]$ is of 12×12^{12} dimensions.

Referring to Eqs. (5.1) and (5.2), the rank of Eq. (5.9) is calculated as below.

$$\text{rank}\left[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \widehat{A}_3, \widehat{A}_4, \widehat{A}_5, \widehat{A}_6, \widehat{A}_7, \widehat{A}_8, \widehat{A}_9, \widehat{A}_{10}, \widehat{A}_{11}\right] = p = 8 \tag{5.10}$$

Since upper and lower sub-inverters of the nine-switch dual-output inverter are both three-phase three-wire inverters, only four state variables per inverter are independent. Equation (5.10) indicates that the nine-switch dual-output inverter is state controllable.

5.2.3 6-*Mode SVPWM*

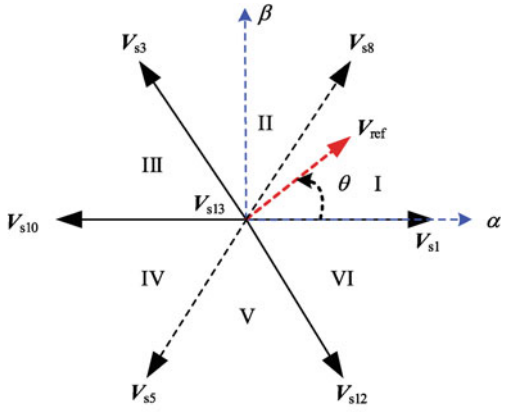
According to Eq. (2.8), it can be concluded that when the operating mode number $m = 4$, up to 16 control variables can be formed, which is greater than the number of state variables of the nine-switch inverter. Therefore, the minimum number of operating modes to control the nine-switch inverter is 4. However, considering the switching constraints of the upper and lower sub-inverters in Table 5.3, the upper and lower sub-inverters should be controlled independently, in order to simplify the control strategy. Therefore, the 3-mode SVPWM for the three-phase four-wire inverter can be used to modulate the upper and lower sub-inverters, respectively, which results in a 6-mode SVPWM for the nine-switch dual-output inverter.

Therefore, two symmetric 6-mode SVPWM methods can be constructed [5]. (1) 6-mode SVPWM I is shown in Fig. 5.4a, in which $\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$ for the upper sub-inverter and $\vec{V}_{s8}$, $\vec{V}_{s10}$, $\vec{V}_{s12}$ for the lower one; (2) 6-mode SVPWM II is shown

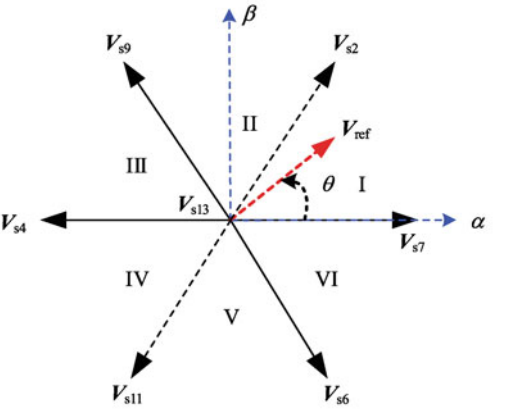
in Fig. 5.4b, in which $\vec{V}_{s2}$, $\vec{V}_{s4}$, $\vec{V}_{s6}$ for the upper sub-inverter and $\vec{V}_{s7}$, $\vec{V}_{s9}$, $\vec{V}_{s11}$ for the lower one.

Take 6-mode SVPWM II as an example to illustrate the switching process. Assuming that synchronous modulation is adopted and only one switch in each leg is turned ON or OFF at one time, the switching sequences as shown in Tables 5.4 and 5.5 can be designed. Table 5.4 lists the upper–lower inverter switching strategy while Table 5.5 lists the lower–upper inverter switching strategy. Comparing with the conventional SVPWM in Table 5.2, the number of switching times reduced by two-third, and the equivalent switching frequency is only one-third of that of the conventional SVPWM accordingly.

In addition, the conventional SVPWM generally divides one cycle into two sections to control upper and lower inverters, respectively. That is, the upper sub-inverter



(a) 6-mode SVPWM I ($\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$, $\vec{V}_{s8}$, $\vec{V}_{s10}$, $\vec{V}_{s12}$)



(b) 6-mode SVPWM II ($\vec{V}_{s2}$, $\vec{V}_{s4}$, $\vec{V}_{s6}$, $\vec{V}_{s7}$, $\vec{V}_{s9}$, $\vec{V}_{s11}$)

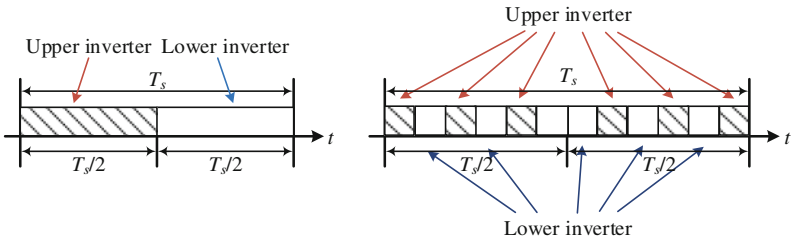
Fig. 5.4 Diagrams of 6-mode SVPWM methods for nine-switch dual-output inverter

Table 5.4 Switching sequences of the upper–lower inverter strategy within 2 cycles

Upper sub-inverter	Lower sub-inverter	Switching sequence	Switching times
Sector I	Sector IV	*u*101-*l*010-111-*u*110-*l*001	4
Sector II	Sector V	*u*110-*l*001-111-*u*011-*l*100	4
Sector III	Sector VI	*u*110-*l*001-111-*u*011-*l*100	4
Sector IV	Sector I	*u*011-*l*100-111-*u*101-*l*010	4
Sector V	Sector II	*u*011-*l*100-111-*u*101-*l*010	4
Sector VI	Sector III	*u*101-*l*010-111-*u*110-*l*001	4
Total			24

Table 5.5 Switching sequences of the lower–upper inverter strategy within two cycles

Upper sub-inverter	Lower sub-inverter	Switching sequence	Switching times
Sector I	Sector IV	*l*001-*u*110-111-*l*010-*u*101	4
Sector II	Sector V	*l*100-*u*011-111-*l*001-*u*110	4
Sector III	Sector VI	*l*100-*u*011-111-*l*001-*u*110	4
Sector IV	Sector I	*l*010-*u*101-111-*l*101-*u*011	4
Sector V	Sector II	*l*010-*u*101-111-*l*101-*u*011	4
Sector VI	Sector III	*l*001-*u*110-111-*l*010-*u*101	4
Total			24



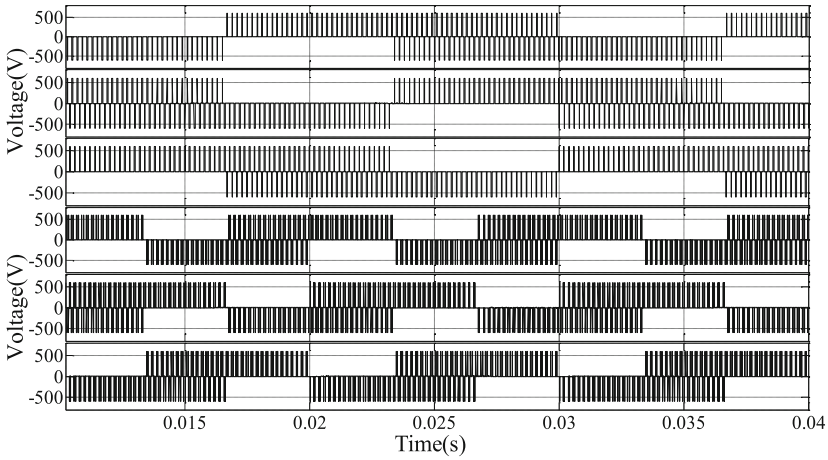
(a) Conventional SVPWM (b) 6-mode SVPWM

Fig. 5.5 Control modes of conventional SVPWM and 6-mode SVPWM

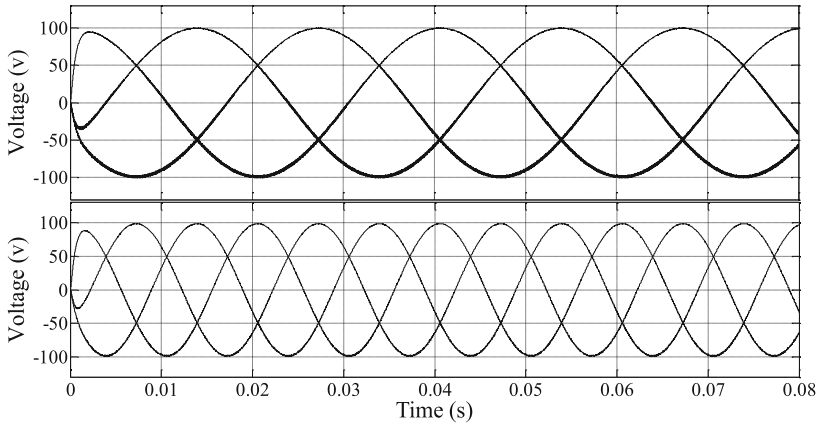
is active in the first section while the lower one is active in the second section, as shown in Fig. 5.5a, which obviously increases the harmonics. However, the upper and lower sub-inverters work alternately under the 6-mode SVPWM, as shown in Fig. 5.5b, which can reduce the harmonics effectively.

5.3 Simulation and Experimental Results

The simulation circuit is built with reference to Fig. 5.1. The circuit parameters are set as follows: $r = 0.2\ \Omega$, $L = 4$ mH, $C = 6.8\ \mu$F. The fundamental frequency of the upper sub-inverter is set to 25 Hz, and that of the lower one is set to 50 Hz. The carrier frequency of the inverter is 10 kHz. According to the switching sequence in Table 5.4, the simulation results are obtained as shown in Fig. 5.6.



(a) Output waveforms before filter.



(b) Output waveforms after filter.

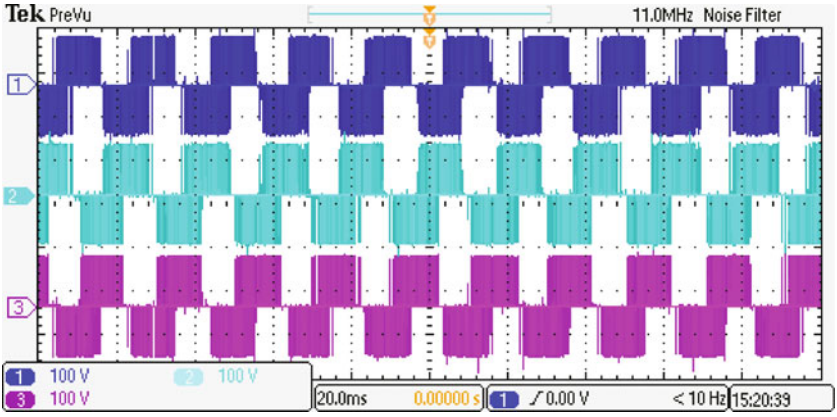
Fig. 5.6 Simulation waveforms of the nine-switch dual-output inverter under 6-mode SVPWM (above: upper sub-inverter; below: lower sub-inverter)

Table 5.6 Prototype parameters of the nine-switch dual-output inverter

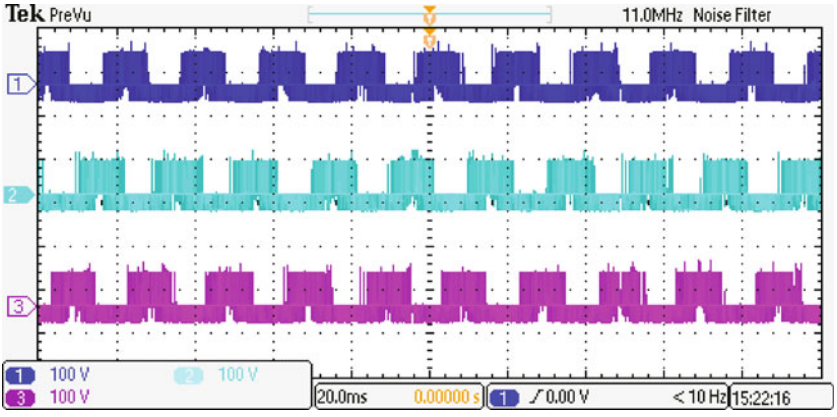
R (Ω)	L (mH)	C (μF)	Carrier frequency (kHz)	Frequency of upper output (Hz)	Frequency of lower output (Hz)
0.5	1.0	25.0	10.0	50.0	25.0

From the simulation results, the nine-switch inverter can output two three-phase sinusoidal voltages with different frequencies, which verify the aforementioned theoretical analysis of 6-mode SVPWM.

The experimental prototype of the nine-switch dual-output inverter is constructed by using the parameters listed in Table 5.6. The line and phase voltages of the upper sub-inverter are shown in Fig. 5.7, while Fig. 5.8 depicts the phase voltages of both



(a) Line voltages.



(b) Phase voltages.

Fig. 5.7 Output voltages of the upper sub-inverter before LC filter

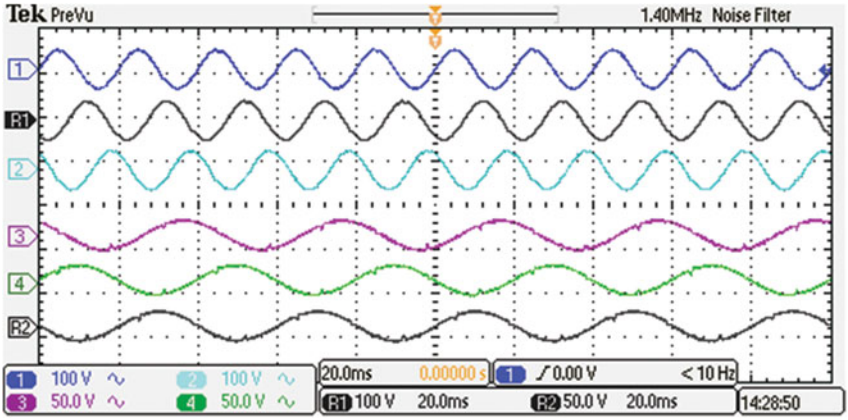


Fig. 5.8 Output phase voltages of the nine-switch dual-output inverter after LC filter

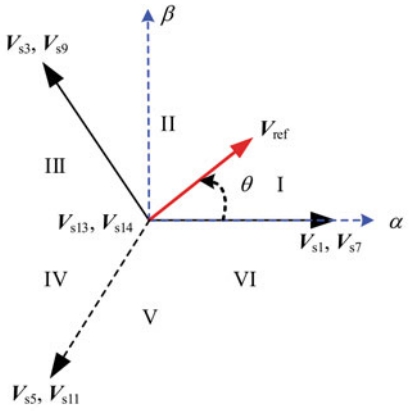
upper and lower sub-inverters after LC filters. The experimental results verify the correctness and feasibility of the proposed 6-mode SVPWM.

5.4 Other *m*-Mode SVPWM for Nine-Switch Dual-Output Inverter

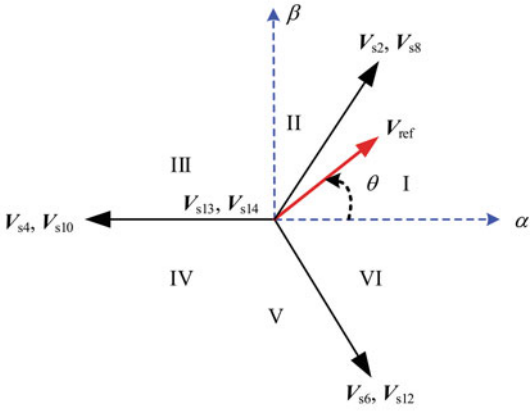
According to the state controllability analysis of the nine-switch dual-output inverter in Sect. 5.2, the inverter can work under other kinds of *m*-mode SVPWM in addition to the 6-mode SVPWM. Except for two kinds of 6-mode SVPWM methods shown in Fig. 5.4, there are two other 6-mode SVPWM methods, which are shown in Fig. 5.9.

Similar to 4-mode SVPWM of the three-phase four-wire inverter, the nine-switch dual-output inverter can also adopt three basic 8-mode SVPWM methods shown in Fig. 5.10a–c. In addition, according to symmetry principle, other kinds of 8-mode SVPWM methods can be formed by removing 4 operating modes from the total 12 operating modes. For example, 8-mode SVPWM IV shown in Fig. 5.10d can be obtained by removing $\vec{V}_{s3}$ and $\vec{V}_{s6}$ of the upper sub-inverter and $\vec{V}_{s7}$ and $\vec{V}_{s10}$ of the lower sub-inverter; 8-mode SVPWM V shown in Fig. 5.10e can be obtained by removing $\vec{V}_{s1}$, $\vec{V}_{s4}$, $\vec{V}_{s9}$ and $\vec{V}_{s12}$. Similarly, other kinds of *m*-mode SVPWM, such as 9-mode, 10-mode or 11-mode SVPWM for the nine-switch dual-output can be proposed according to the actual needs.

Fig. 5.9 Diagrams of other 6-mode SVPWMs



(a) 6-mode SVPWM III ($\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$, $\vec{V}_{s7}$, $\vec{V}_{s9}$, $\vec{V}_{s11}$)

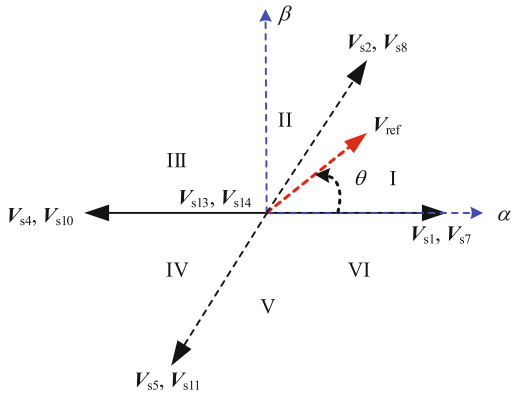


(b) 6-mode SVPWM IV ($\vec{V}_{s2}$, $\vec{V}_{s4}$, $\vec{V}_{s6}$, $\vec{V}_{s8}$, $\vec{V}_{s10}$, $\vec{V}_{s12}$)

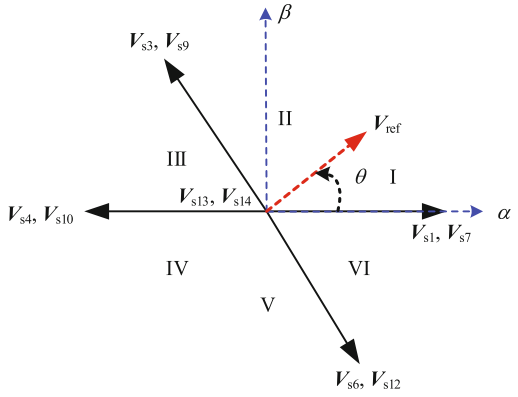
5.5 Summary

This chapter analyzes the *m*-mode controllability of the nine-switch dual-output inverter and puts forward 6-mode SVPWM along with the switching sequences. Theoretical analysis, simulation, and experimental results show that the 6-mode SVPWM of nine-switch dual-output inverter can reduce the number of switching times by two-third compared with the conventional SVPWM, and the switching frequency reduced to one-third accordingly. For the inverters with many operating modes like the nine-switch dual-output inverter, a lot of *m*-mode SVPWM methods can be chosen. The best one can be selected according to actual needs, thereby improving the overall performance of the inverter.

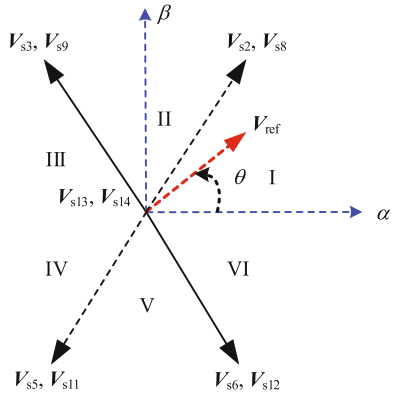
Fig. 5.10 Diagrams of 8-mode SVPWMs



(a) *8*-mode SVPWM I.

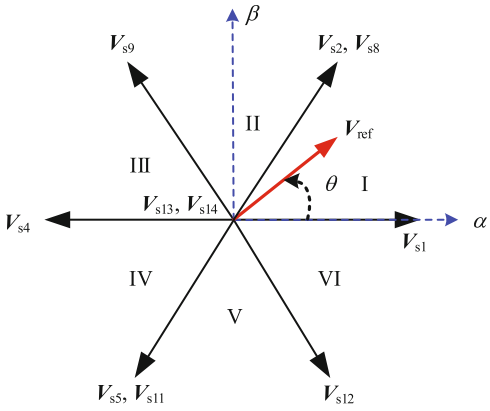


(b) *8*-mode SVPWM II.

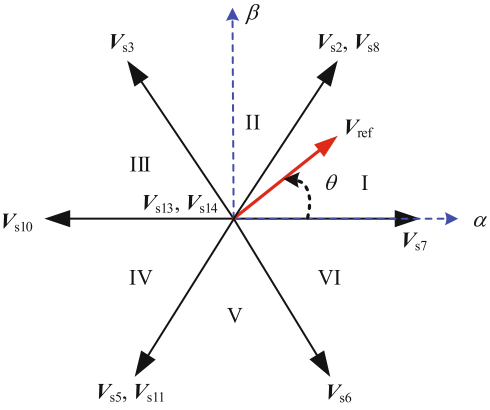


(c) *8*-mode SVPWM III.

Fig. 5.10 (continued)



(d) *8*-mode SVPWM IV.



(e) *8*-mode SVPWM V.

References

1. Kominami T, Fujimoto Y (2007) A novel nine-switch inverter for independent control of two three-phase loads. In: IEEE industry applications annual meeting, pp 2346–2350
2. Wang M, Tian K (2008) A nine-switch three-level inverter for electric vehicle applications. In: IEEE vehicle power and propulsion conference, pp 1–5
3. Dehnavi SMD, Mohamadian M, Yazdian A et al (2010) Space vectors modulation for nine-switch converters. IEEE Trans Power Electron 25(6):1488–1496
4. Aganah K, Karugaba S, Ojo O (2012) Space vector and carrier-based PWM modulation schemes for maximum utilization of voltage sources of a nine-switch converter. In: Energy conversion congress and exposition, pp 2521–2528
5. Li X, Qu L, Zhang B et al (2018) A simplified modulation strategy of nine-switch inverter to cut off half of switching modes. IEEE Access 6:7254–7261

Chapter 6
6-Mode SVPWM for Five-Leg Dual-Output Inverter

Similar to the nine-switch dual-output inverter, the five-leg dual-output inverter is also one of the multi-load inverters. Unlike the nine-switch dual-output inverter consisting of upper and lower inverters, the five-leg dual-output inverter is composed of left and right inverters with more flexible control. In this chapter, the state controllability of the five-leg dual-output inverter will be analyzed systematically, and the corresponding 6-mode SVPWM method will be put forward. Furthermore, the switching sequence and operating characteristics of 6-mode SVPWM will be studied, which provides a novel modulation method for the five-leg dual-output inverter.

6.1 Operating Principle of Five-Leg Dual-Output Inverter

The topology of the five-leg dual-output inverter is shown in Fig. 6.1 [1]. It consists of five phase legs and can be divided into left and right inverters. The left sub-inverter supplying power to load #1 is composed of VT_1, VT_3, VT_5, VT_2, VT_4, and VT_6, while the right sub-inverter supplying power to load #2 is composed of VT_5, VT_7, VT_9, VT_6, VT_8, and VT_{10}. The intermediate leg consisting of VT_5 and VT_6 is shared by the left and right sub-inverters. As a result, the five-leg dual-output inverter has one less leg than two independent inverters, which means two switching devices are saved.

When the five-leg dual-output inverter operates under conventional SVPWM, it can be regarded as two independent three-phase inverters. When one inverter is active, the other one is inactive and output zero voltage vector, which means that two inverters work alternatively to achieve decoupled output. Therefore, the five-leg dual-output inverter has 14 operating modes in total, and the corresponding voltage vectors are listed in Table 6.1, which can be represented by the binary combination of the upper switch in each leg. In order to distinguish the left and right inverters, letter "*l*" or "*r*" is put before the binary representation, where "*l*" denotes the left sub-inverter and "*r*" denotes the right sub-inverter [2, 3]. The equivalent circuits of

B. Zhang and D. Qiu, *m-Mode SVPWM Technique for Power Converters*, CPSS Power Electronics Series, https://doi.org/10.1007/978-981-13-1382-0_6

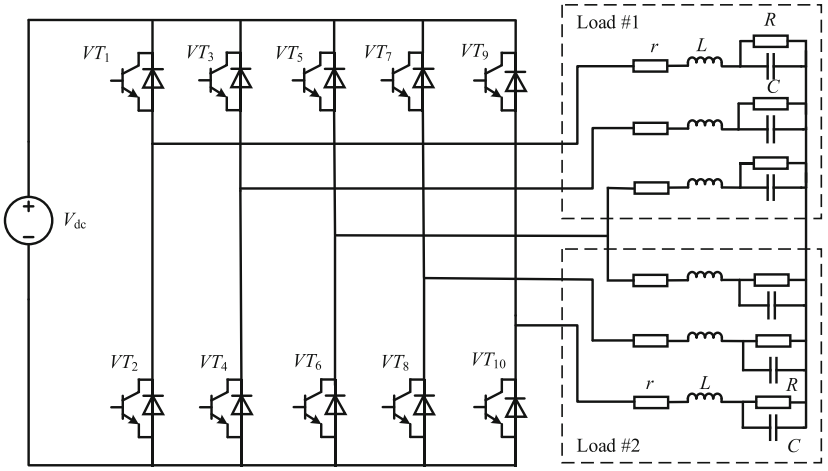


Fig. 6.1 Five-leg dual-output inverter

the five-leg dual-output inverter corresponding to 14 operating modes are shown in Fig. 6.2.

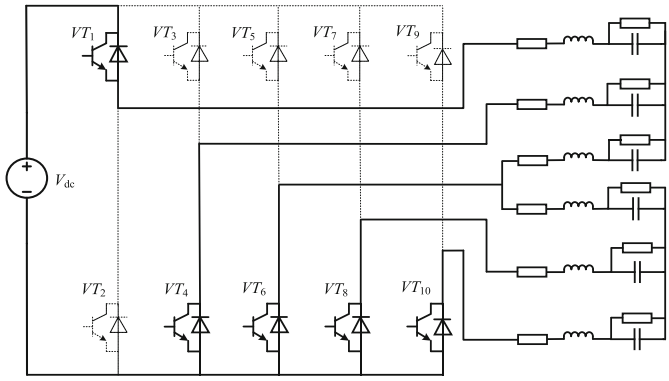
In the conventional SVPWM strategy, each operating mode in Fig. 6.2 can be represented by a voltage space vector in the complex plane. Figure 6.3 shows the distribution of 14 basic voltage space vectors on the complex plane, which is divided into six sectors by the nonzero voltage space vectors ($\vec{V}_{s1}$ to $\vec{V}_{s12}$). Among 12 nonzero voltage space vectors, $\vec{V}_{s1}$ to $\vec{V}_{s6}$ correspond to the left sub-inverter, while $\vec{V}_{s7}$ to $\vec{V}_{s12}$ correspond to the right sub-inverter.

In order to ensure the completely decoupled of the left and right sub-inverters, one switching cycle is generally divided into two parts, and the left and right sub-inverters operate in one-half of the switching cycle, respectively. Table 6.2 lists the switching sequences of conventional SVPWM for the five-leg dual-output inverter.

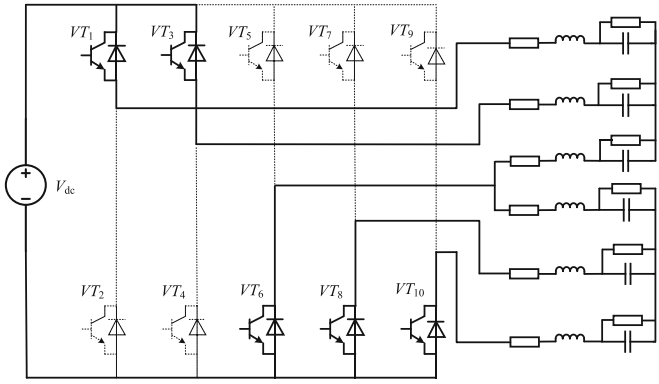
Since the left and right sub-inverters of the five-leg dual-output inverter work independently, the duration time of each vector needs to be calculated separately, which obviously increases the calculation amount of the conventional SVPWM algorithm. In addition, the number of combined sectors of the left and right sub-inverters is up to 36, and as a result, the complexity of the SVPWM algorithm is significantly increased.

Table 6.1 Operating modes of the five-leg dual-output inverter

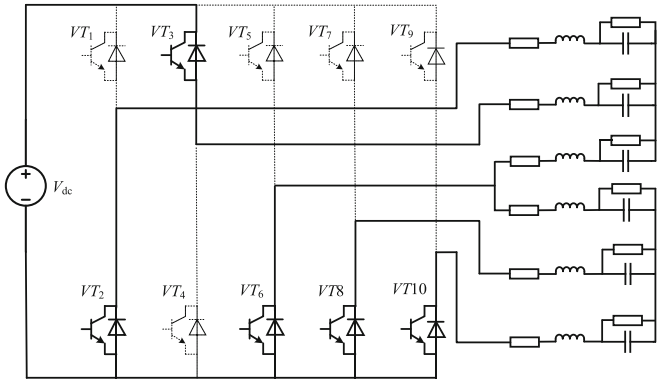
Mode	VT_1	VT_2	VT_3	VT_4	VT_5	VT_6	VT_7	VT_8	VT_9	VT_{10}	Voltage vector	Binary representation
1	ON	OFF	OFF	ON	OFF	ON	OFF	ON	OFF	ON	$\vec{V}_{s1}$	*l*100
2	ON	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	ON	$\vec{V}_{s2}$	*l*110
3	OFF	ON	ON	OFF	OFF	ON	OFF	ON	OFF	ON	$\vec{V}_{s3}$	*l*010
4	OFF	ON	ON	OFF	ON	OFF	ON	OFF	ON	OFF	$\vec{V}_{s4}$	*l*011
5	OFF	ON	OFF	ON	ON	OFF	ON	OFF	ON	OFF	$\vec{V}_{s5}$	*l*001
6	ON	OFF	OFF	ON	ON	OFF	ON	OFF	ON	OFF	$\vec{V}_{s6}$	*l*101
7	ON	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	ON	$\vec{V}_{s7}$	*r*100
8	ON	OFF	ON	OFF	ON	OFF	ON	OFF	OFF	ON	$\vec{V}_{s8}$	*r*110
9	OFF	ON	OFF	ON	OFF	ON	ON	OFF	OFF	ON	$\vec{V}_{s9}$	*r*010
10	OFF	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	$\vec{V}_{s10}$	*r*011
11	OFF	ON	OFF	ON	OFF	ON	OFF	ON	ON	OFF	$\vec{V}_{s11}$	*r*001
12	ON	OFF	ON	OFF	ON	OFF	OFF	ON	ON	OFF	$\vec{V}_{s12}$	*r*101
13	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	$\vec{V}_{s13}$	111
14	OFF	ON	OFF	ON	OFF	ON	OFF	ON	OFF	ON	$\vec{V}_{s14}$	000



(a) Operating mode 1 (*l*100)

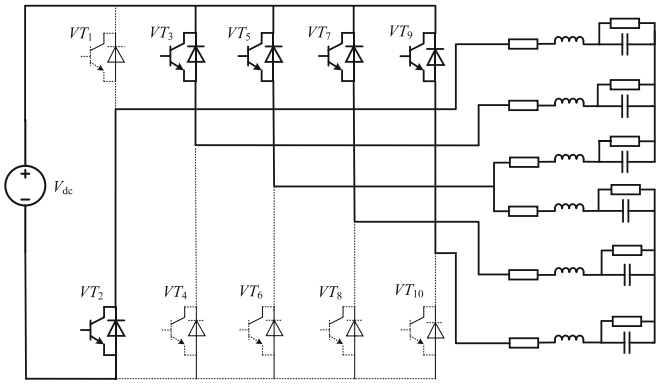


(b) Operating mode 2 (*l*110)

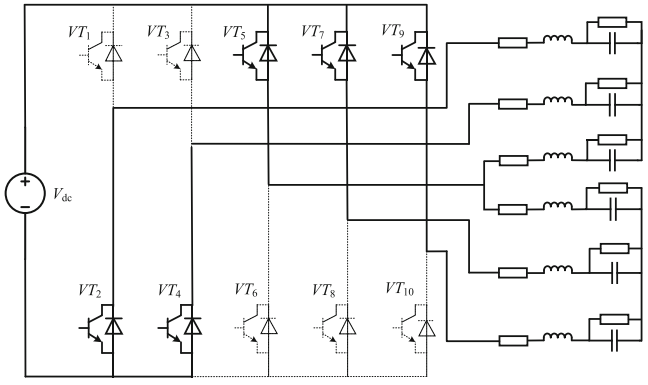


(c) Operating mode 3 (*l*010)

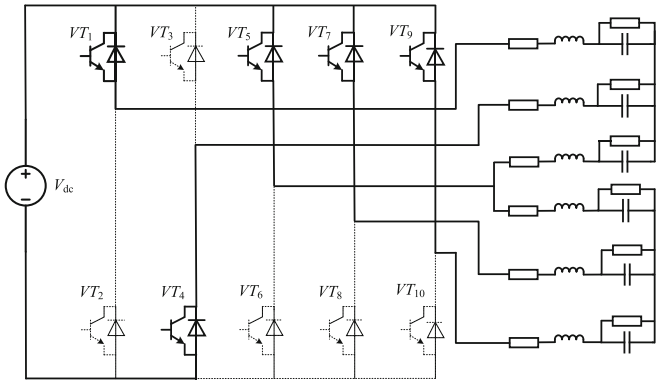
Fig. 6.2 Equivalent circuits of the five-leg dual-output inverter



(d) Operating mode 4 (*l*011)

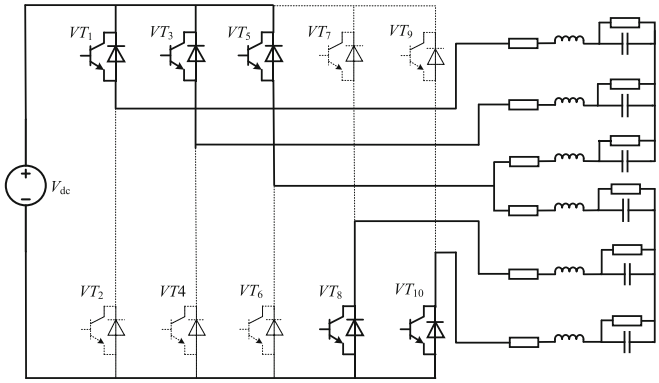


(e) Operating mode 5 (*l*001)

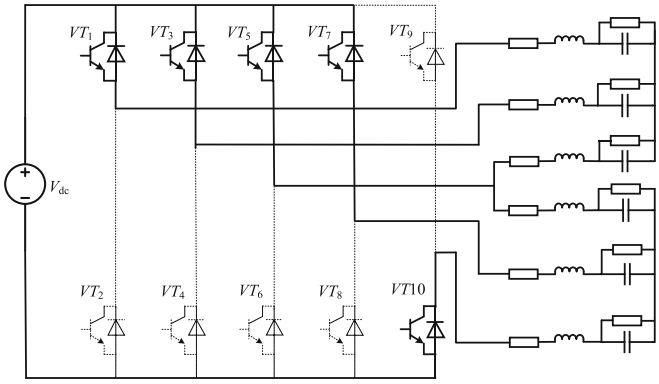


(f) Operating mode 6 (*l*101)

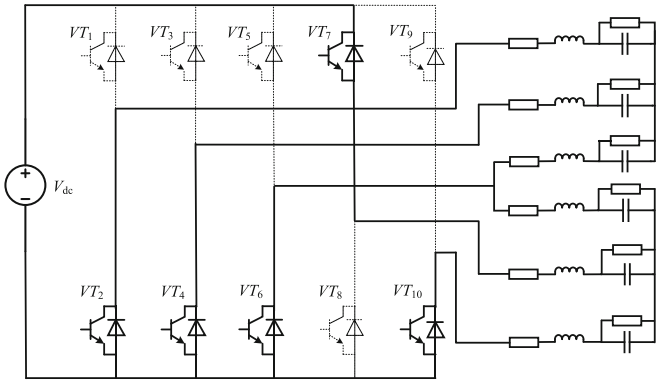
Fig. 6.2 (continued)



(g) Operating mode 7 ($r100$)

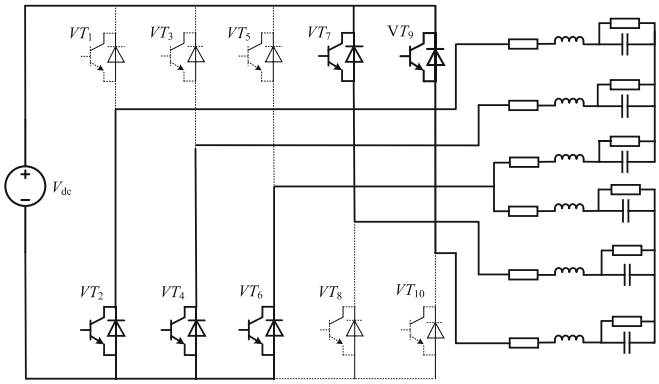


(h) Operating mode 8 ($r110$)

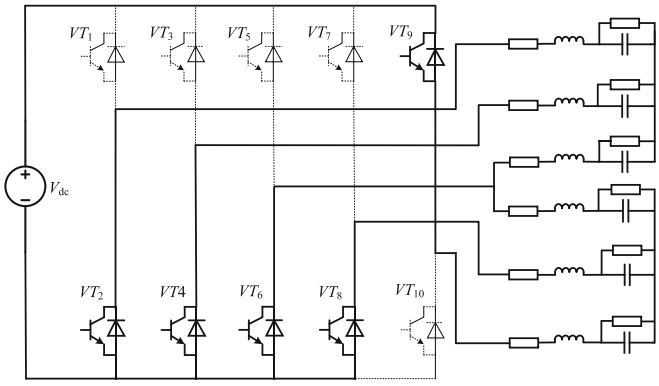


(i) Operating mode 9 ($r010$)

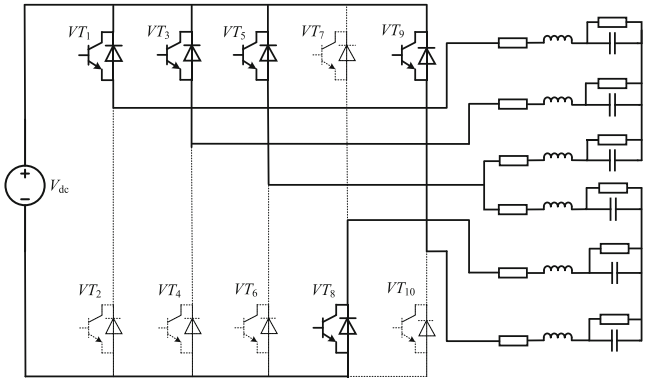
Fig. 6.2 (continued)



(j) Operating mode 10 (r011)

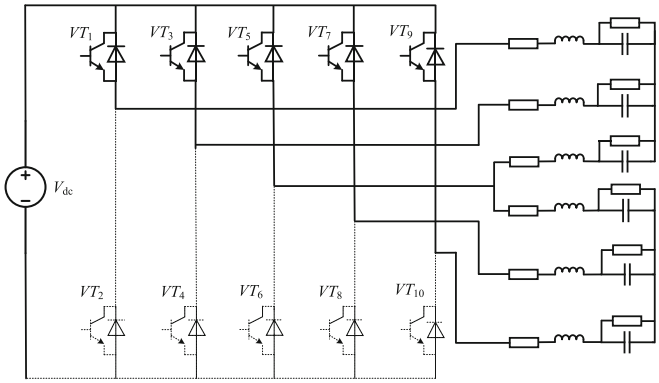


(k) Operating mode 11 (r001)

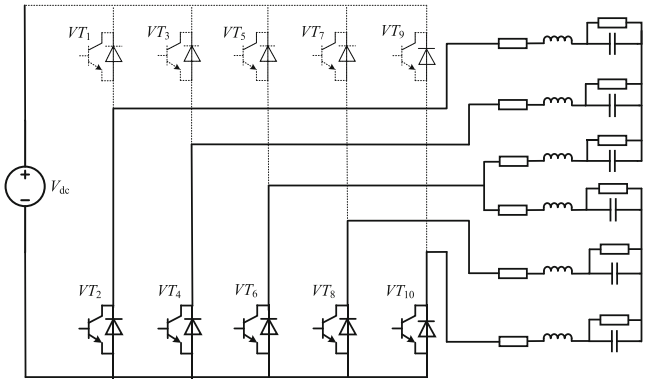


(l) Operating mode 12 (r101)

Fig. 6.2 (continued)



(m) Operating mode 13 (111)



(n) Operating mode 14 (000)

Fig. 6.2 (continued)

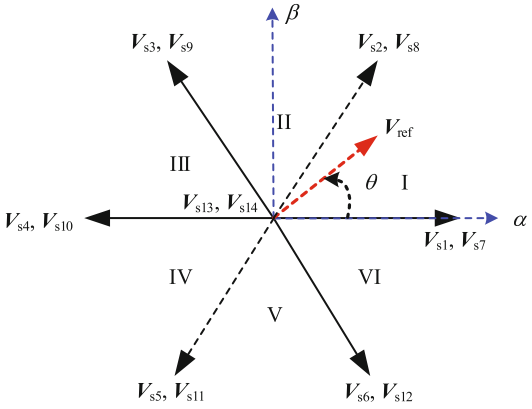


Fig. 6.3 Distribution of basic voltage space vectors

Table 6.2 Switching sequences of conventional SVPWM

Sector	Left sub-inverter	Right sub-inverter	Switching times
I	000-l100-l110-111-l110-l100-000	000-*r*100-*r*110-111-*r*110-*r*100-000	12
II	000-l010-l110-111-l110-l010-000	000-*r*010-*r*110-111-*r*110-*r*010-000	12
III	000-l010-l011-111-l011-l010-000	000-*r*010-*r*011-111-*r*011-*r*010-000	12
IV	000-l001-l011-111-l011-l001-000	000-*r*001-*r*011-111-*r*011-*r*001-000	12
V	000-l001-l101-111-l101-l001-000	000-*r*001-*r*101-111-*r*101-*r*001-000	12
VI	000-l100-l101-111-l101-l100-000	000-*r*100-*r*101-111-*r*101-*r*100-000	12
Total			72

6.2 6-Mode SVPWM Strategy

6.2.1 Switched Linear System Model

Select $x = \left[x_l \; x_r \right]^{\mathrm{T}}$ as the state variable matrix of the five-leg dual-output inverter, where x_l is the state variables of the left sub-inverter and x_r is that of the right sub-inverter. Let the output inductor currents and capacitor voltages of two loads be the state variables, then $x_l = [i_{al}, i_{bl}, i_{cl}, u_{al}, u_{bl}, u_{cl}]^{\mathrm{T}}$ and $x_r = [i_{ar}, i_{br}, i_{cr}, u_{ar}, u_{br}, u_{cr}]^{\mathrm{T}}$. Assuming that the load parameters of the five-leg dual-output inverter in Fig. 6.1 are the same, the coefficient matrixes of the switched linear system model of the five-leg dual-output inverter can be obtained as below:

$$A_1 = \cdots = A_{14} = \begin{bmatrix} A_{a1} & 0 \\ 0 & A_{a2} \end{bmatrix} \tag{6.1}$$

$$\left[B_1 \; B_2 \; \cdots \; B_{14} \right] = \begin{bmatrix} B_{a1} & 0 \\ 0 & B_{a2} \end{bmatrix} \tag{6.2}$$

$$C_1 = \cdots = C_{14} = \begin{bmatrix} C_{a1} & 0 \\ 0 & C_{a2} \end{bmatrix} \tag{6.3}$$

$$A_{a1} = A_{a2} = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} \end{bmatrix} \tag{6.4}$$

$$B_{a1} = B_{a2} = \begin{bmatrix} \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} \\ -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} \\ -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{6.5}$$

$$C_{a1} = \begin{bmatrix} 0\,0\,0\,1\,0\,0\,0\,0\,0\,0\,0\,0 \\ 0\,0\,0\,0\,1\,0\,0\,0\,0\,0\,0\,0 \\ 0\,0\,0\,0\,0\,1\,0\,0\,0\,0\,0\,0 \end{bmatrix} \tag{6.6}$$

$$C_{a2} = \begin{bmatrix} 0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,1\,0\,0 \\ 0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,1\,0 \\ 0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,0\,1 \end{bmatrix} \tag{6.7}$$

6.2.2 m-*Mode Controllability*

Corresponding to Eq. (2.6), the matrix to analyze the state controllability of the five-leg dual-output inverter can be constructed as follows:

$$\left[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \widehat{A}_3, \widehat{A}_4, \widehat{A}_5, \widehat{A}_6, \widehat{A}_7, \widehat{A}_8, \widehat{A}_9, \widehat{A}_{10}, \widehat{A}_{11}\right] \tag{6.8}$$

where $\widehat{B} = [B_1, B_2, \ldots, B_{12}]$ is a matrix of 12×12 dimensions; $\widehat{A}_1 = \left[A_1\widehat{B}, A_2\widehat{B}, \ldots, A_{12}\widehat{B}\right]$ is of 12×12^2 dimensions; $\widehat{A}_2 = \left[A_1\widehat{A}_1, A_2\widehat{A}_1, \cdots, A_{12}\widehat{A}_1\right]$ is of 12×12^3 dimensions; $\widehat{A}_3 = \left[A_1\widehat{A}_2, A_2\widehat{A}_2, \ldots, A_{12}\widehat{A}_2\right]$ is of 12×12^4 dimensions; …; $\widehat{A}_{11} = \left[A_1\widehat{A}_{10}, A_2\widehat{A}_{10}, \ldots, A_{12}\widehat{A}_{10}\right]$ is of 12×12^{12} dimensions.

Referring to Eqs. (6.1)–(6.5), the rank of Eq. (6.8) is calculated as below:

$$\text{rank}\left[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \widehat{A}_3, \widehat{A}_4, \widehat{A}_5, \widehat{A}_6, \widehat{A}_7, \widehat{A}_8, \widehat{A}_9, \widehat{A}_{10}, \widehat{A}_{11}\right] = p = 8 \tag{6.9}$$

Since both left and right sub-inverters in the five-leg dual-output inverter can be considered as the three-phase three-wire inverter, only four variables per inverter are independent. Therefore, the matrix in Eq. (6.8) is full-rank, which indicates that five-leg dual-output inverter is state controllable.

6.2.3 6-*Mode SVPWM*

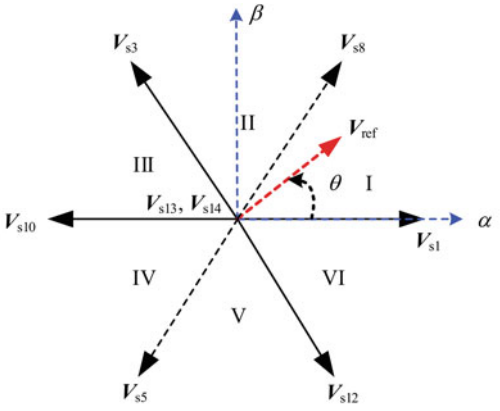
According to Eq. (2.8), it can be concluded that a maximum of 16 control variables can be formed when 4 operating modes are used, which is greater than the number of state variables. Therefore, the minimum number of operating modes for SVPWM is 4.

Since the left and right sub-inverters of the five-leg dual-output inverter can be independently controlled, the *m*-mode SVPWM for the three-phase three-wire inverter can be used as a reference. The left and right sub-inverters can adopt the 3-mode SVPWM, respectively, which means that the five-leg dual-output inverter can operate under 6-mode SVPWM.

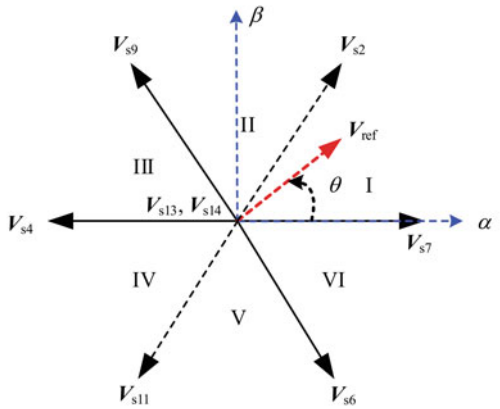
Therefore, two kinds of vector-symmetric 6-mode SVPWM can be obtained. In 6-mode SVPWM I shown in Fig. 6.4a, the left sub-inverter adopts $\vec{V}_{s1}$, $\vec{V}_{s3}$ and $\vec{V}_{s5}$, while the right one chooses $\vec{V}_{s8}$, $\vec{V}_{s10}$ and $\vec{V}_{s12}$. In 6-mode SVPWM II shown in Fig. 6.4b, the left sub-inverter adopts $\vec{V}_{s2}$, $\vec{V}_{s4}$ and $\vec{V}_{s6}$, while the right one chooses $\vec{V}_{s7}$, $\vec{V}_{s9}$ and $\vec{V}_{s11}$.

6-mode SVPWM II in Fig. 6.4b is taking as an example to illustrate the switching process. It is assumed that synchronous modulation is adopted, and only one switch in each sub-inverter is turned ON/OFF at one time. Therefore, the switching sequences can be summarized in Tables 6.3 and 6.4, in which Table 6.3 depicts the left–right-inverter switching strategy, while Table 6.4 is the right–left-inverter switching strategy. Compared with the conventional SVPWM in Table 6.2, the number of switching times reduced by 2/3, and the equivalent switching frequency is only 1/3 of the conventional SVPWM switching frequency.

From Tables 6.3 and 6.4, when the five-leg dual-output inverter adopts 6-mode SVPWM, the left and right sub-inverters can work alternately, which effectively reduces the output harmonics compared with the conventional SVPWM.



(a) 6-mode SVPWM I ($\vec{V}_{s1}$, $\vec{V}_{s3}$, $\vec{V}_{s5}$, $\vec{V}_{s8}$, $\vec{V}_{s10}$, $\vec{V}_{s12}$)



(b) 6-mode SVPWM II ($\vec{V}_{s2}$, $\vec{V}_{s4}$, $\vec{V}_{s6}$, $\vec{V}_{s7}$, $\vec{V}_{s9}$, $\vec{V}_{s11}$)

Fig. 6.4 6-mode SVPWMs for five-leg dual-output inverter

Table 6.3 Switching sequences of the left–right-inverter strategy within 2 cycles

Left sub-inverter	Right sub-inverter	Switching sequence	Switching times
I	IV	*l*101-*r*010-000-*l*110-*r*001	4
II	V	*l*110-*r*001-000-*l*011-*r*100	4
III	VI	*l*110-*r*001-000-*l*011-*r*100	4
IV	I	*l*011-*r*100-000-*l*101-*r*010	4
V	II	*l*011-*r*100-000-*l*101-*r*010	4
VI	III	*l*101-*r*010-000-*l*110-*r*001	4
Total			24

Table 6.4 Switching sequence of the right–left-inverter strategy within 2 cycles

Left sub-inverter	Right sub-inverter	Switching sequence	Switching times
I	IV	*r*001-*l*110-000-*r*010-*l*101	4
II	V	*r*100-*l*011-000-*r*001-*l*110	4
III	VI	*r*100-*l*011-000-*r*001-*l*110	4
IV	I	*r*010-*l*101-000-*r*101-*l*011	4
V	II	*r*010-*l*101-000-*r*101-*l*011	4
VI	III	*r*001-*l*110-000-*r*010-*l*101	4
Total			24

6.3 Simulation and Experimental Results

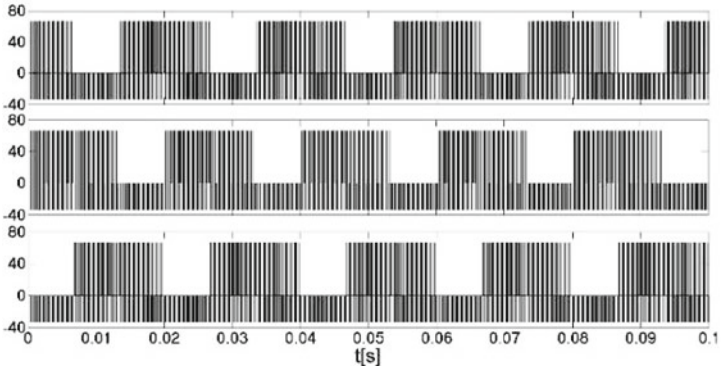
The simulation circuit of the five-leg dual-output inverter is the same as Fig. 6.1. The parameters are set as follows: $V_{dc} = 100$ V, $r = 0.2\ \Omega$, $L = 4$ mH, $C = 10\ \mu$F, the output frequency of left sub-inverter is 50 Hz, and that of the right one is 25 Hz. Based on the switching sequence in Table 6.3, the simulation results are obtained in Figs. 6.5, 6.6, 6.7, and 6.8.

It can be seen from the simulation waveforms that the five-leg dual-output inverter can work normally under 6-mode SVPWM and output two desired sinusoidal signals of different frequencies, which verifies the correctness of the above theoretical analysis.

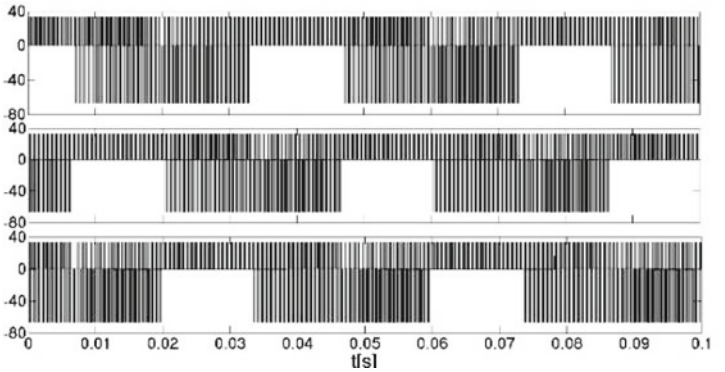
In order to further verify the operating characteristics of the 6-mode SVPWM, the experimental verification was carried out under the same parameters. The experimental waveforms are shown in Figs. 6.9, 6.10, 6.11, and 6.12. It is found that two three-phase loads can operate at different frequencies under the proposed 6-mode SVPWM, which confirms the independent modulation of left and right sub-inverters.

6.4 Comparison with Conversional SVPWM

The harmonic analysis of two load currents outputted by the five-leg dual-output inverter is shown in Table 6.5. It can be found that the harmonic contents of two load currents are quite close and can meet the actual requirements. Compared with the existing conventional SVPWM, it is found that the harmonic contents of the 6-mode SVPWM are greater, but the gap between the 6-mode SVPWM and the conventional SVPWM will shrink as the switching frequency increases.



(a) Left sub-inverter.

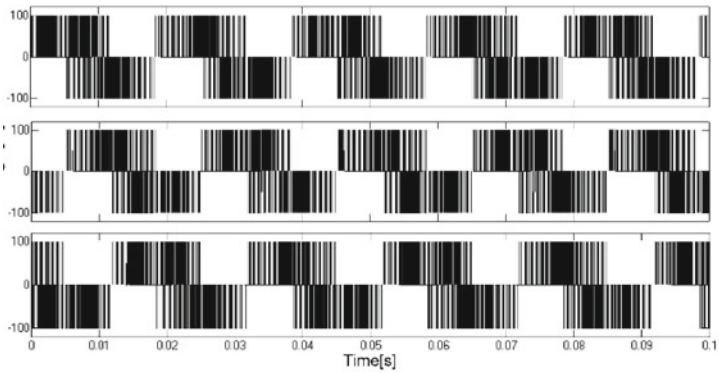


(b) Right sub-inverter.

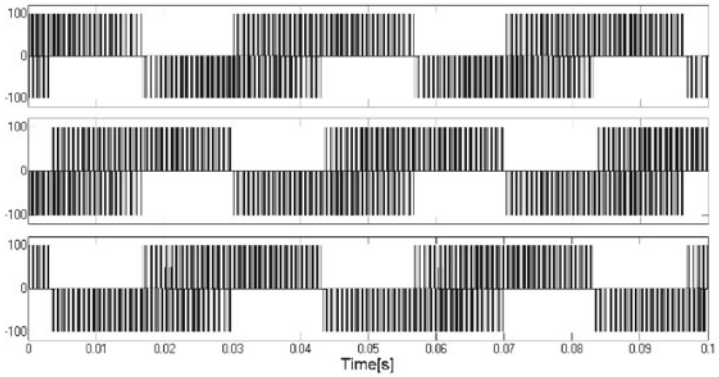
Fig. 6.5 Simulation waveforms of phase voltage under 6-mode SVPWM (before filter)

Table 6.5 Analysis of harmonic contents

Control strategy	Sub-inverter	Harmonic content		
		10 kHz	15 kHz	20 kHz
6-mode SVPWM I (%)	Left	3.48	1.69	1.00
	Right	3.66	1.95	1.06
6-mode SVPWM II (%)	Left	3.48	1.69	0.99
	Right	3.49	1.73	1.03
Conventional SVPWM (%)	Left	0.62	0.29	0.22
	Right	0.64	0.32	0.20



(a) Left sub-inverter.



(b) Right sub-inverter.

Fig. 6.6 Simulation waveforms of line voltage under 6-mode SVPWM (before filter)

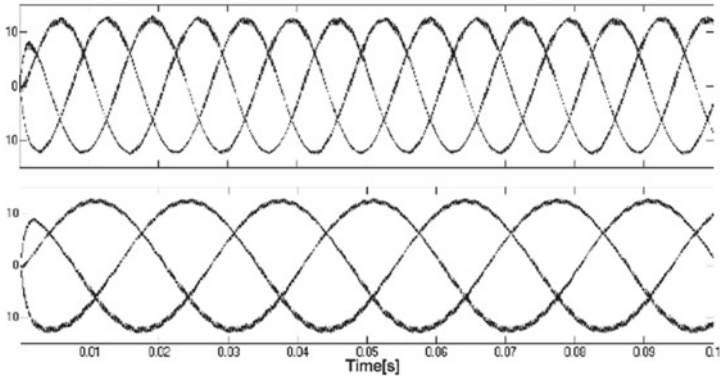


Fig. 6.7 Simulation waveforms of line voltage after filter (above: left sub-inverter, below: right sub-inverter)

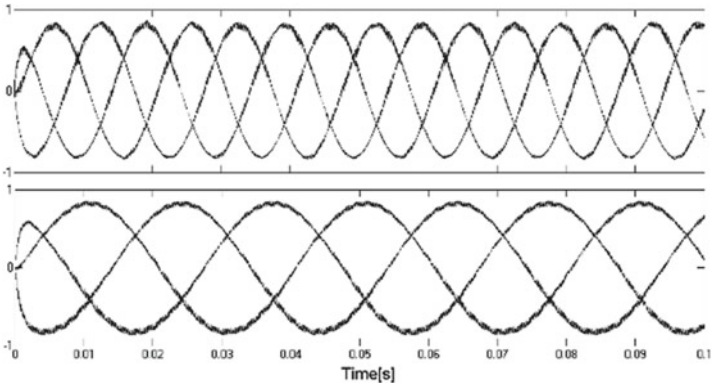
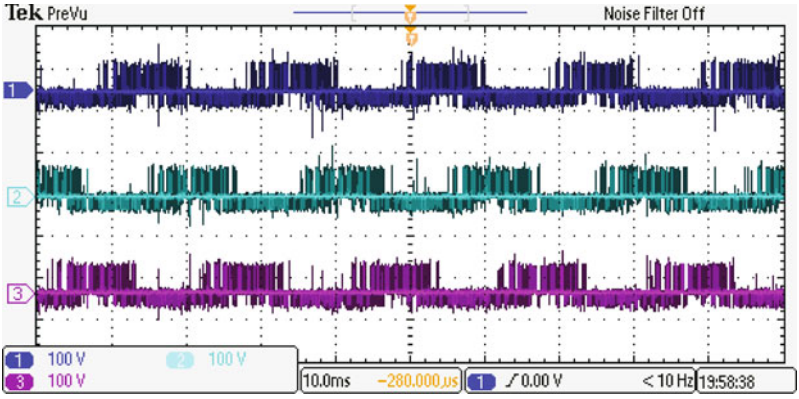
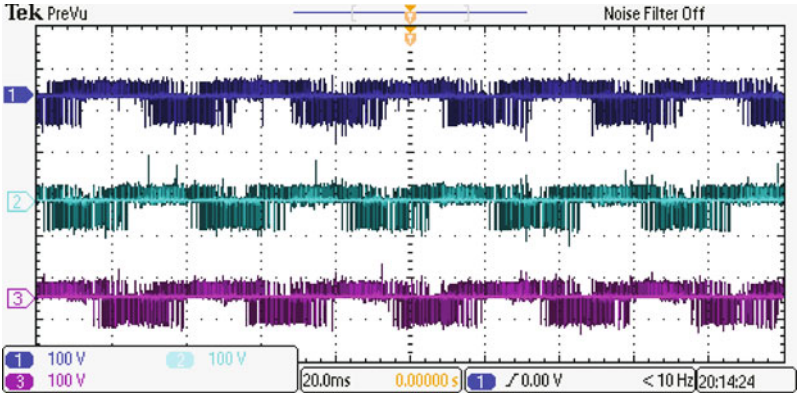


Fig. 6.8 Simulation waveforms of phase current under 6-mode SVPWM (above: left sub-inverter, below: right sub-inverter)

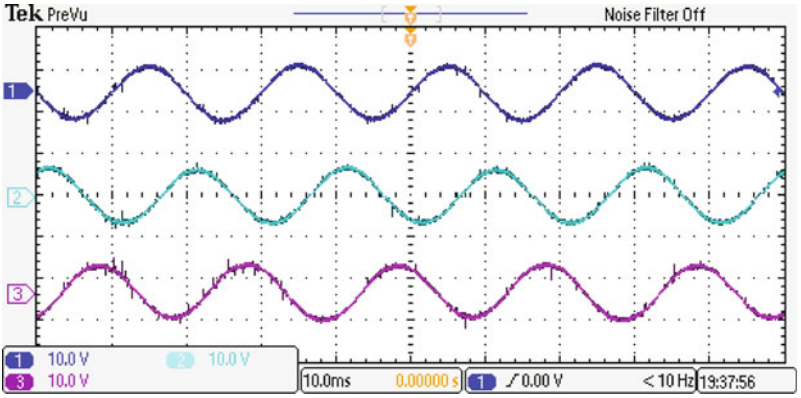


(a) Left sub-inverter.

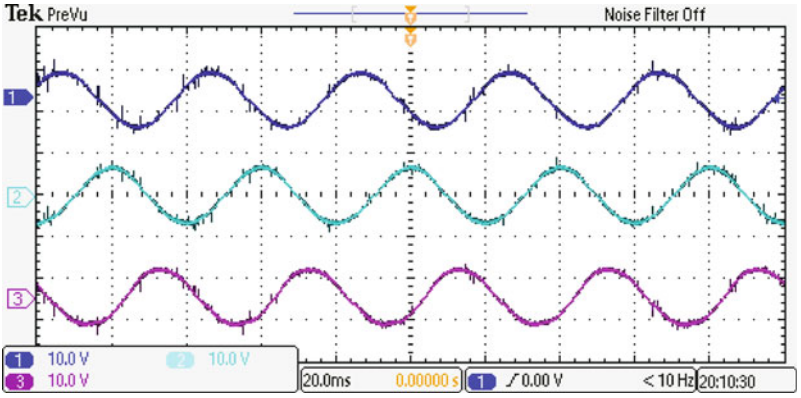


(b) Right sub-inverter.

Fig. 6.9 Experimental waveforms of phase voltage under 6-mode SVPWM (before filter)



(a) Left sub-inverter.



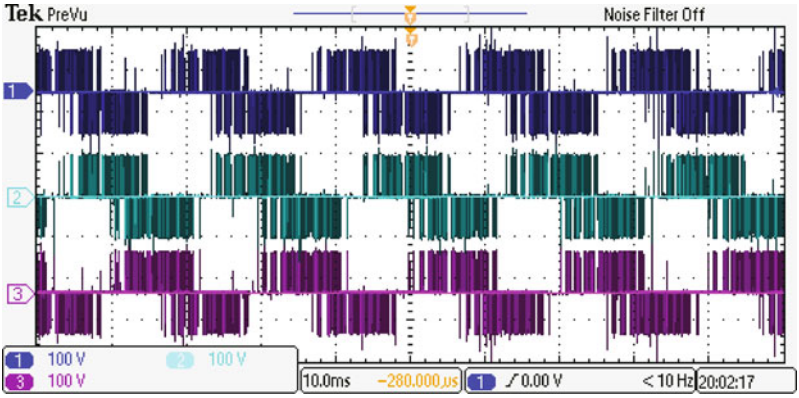
(b) Right sub-inverter.

Fig. 6.10 Experimental waveforms of phase voltage under 6-mode SVPWM (after filter)

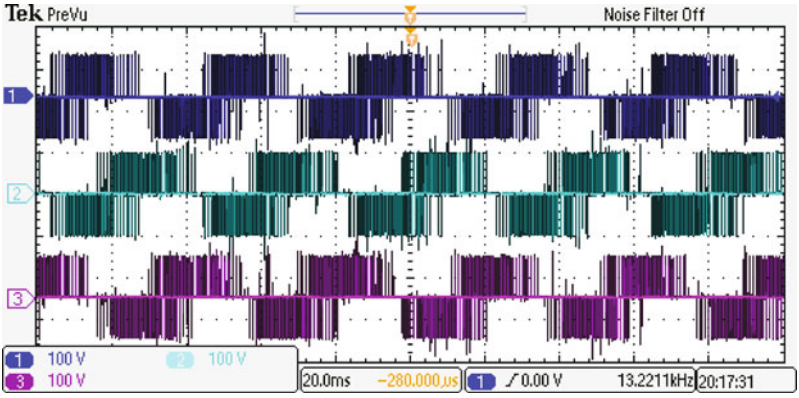
Table 6.6 Analysis of switching times under different switching frequencies

Frequency (kHz)	6-mode SVPWM I	6-mode SVPWM II	Conventional SVPWM
10	15,358	15,356	52,144
15	23,094	23,058	77,310
20	30,578	30,686	101,604

The number of switching times of the five-leg dual-output inverter under different modulation strategies is counted within the period of 0.2 s. The results are shown in Table 6.6. With the increase of the switching frequency, the number of switching times under conventional SVPWM is much greater than that of 6-mode SVPWM, and the gap becomes larger as the frequency increases.



(a) Left sub-inverter.

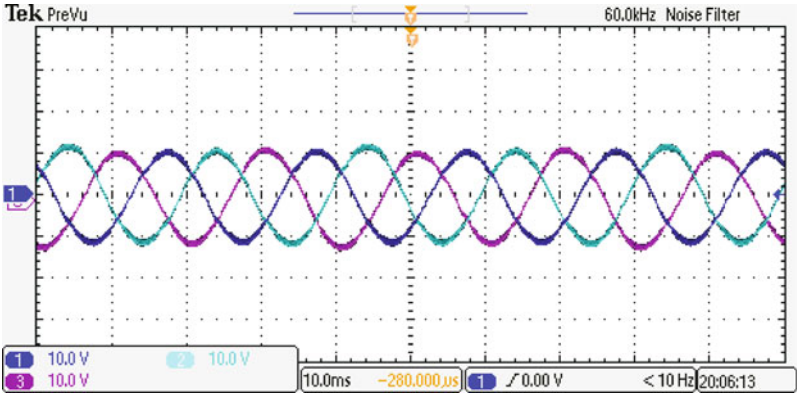


(b) Right sub-inverter.

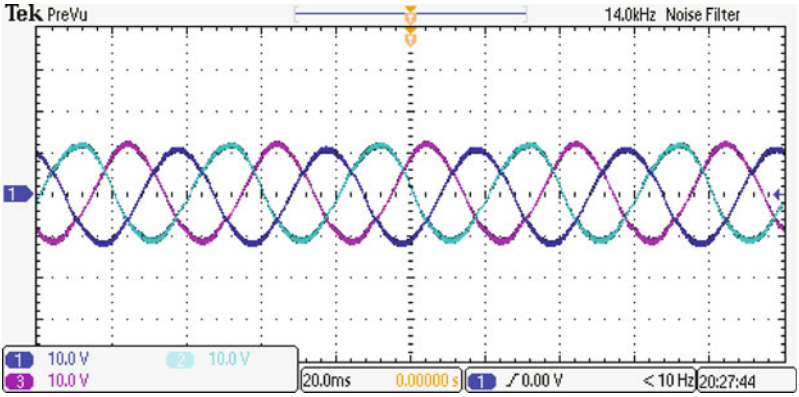
Fig. 6.11 Experimental waveforms of line voltage under 6-mode SVPWM (before filter)

6.5 Summary

This chapter analyzed the *m*-mode controllability of the five-leg dual-output inverter and put forward the 6-mode SVPWM methods along with the corresponding switching sequences. Theoretical analysis, simulation, and experimental results show that the five-leg dual-output inverter operating under 6-mode SVPWM can reduce the number of switching times by 2/3 compared with conventional SVPWM, and the equivalent switching frequency is only 1/3 of the conventional one. At the same actual switching frequency, the harmonic contents of the five-leg dual-output inverter under the 6-mode SVPWM are comparable to those of the conventional SVPWM, which proves the practicability of the 6-mode SVPWM.



(a) Left sub-inverter.



(b) Right sub-inverter.

Fig. 6.12 Experimental waveforms of line voltage under 6-mode SVPWM (after filter)

References

1. Jones M, Vukosavic SN, Dujic D et al (2008) Five-leg inverter PWM technique for reduced switch count two-motor constant power applications. IET Electr Power Appl 2(5):275–287
2. Hizume M (2003) Independent vector control of parallel-connected two induction motors by a five-leg inverter. In: 10th European conference on power electronics and applications, vol 778
3. Oka K, Matsuse K (2009) PWM technique of five-leg inverter applying two-arm modulation. IEEJ Trans Ind Appl 129:811–816

Chapter 7
m-Mode SVPWM for Multilevel Inverter

Compared with the aforementioned two-level inverter, the multilevel inverter can further reduce the harmonics of the output voltage and current. However, the structure of the multilevel inverter is more complicated, which makes the design of the SVPWM switching sequences more difficult. Besides, the issues such as capacitor voltage balance should also be considered. Therefore, the *m*-mode SVPWM is more practical for the multilevel inverters. In this chapter, the topologies and the existing SVPWM of the multilevel inverter are analyzed first. Then, taking the diode-clamped three-level inverter as an example, the state controllability is studied and several *m*-mode SVPWMs of the diode-clamp three-level inverter are proposed. Furthermore, the switching sequences and operating characteristics of the diode-clamp three-level inverter are studied, in order to achieve the purpose of reducing the switching frequency and calculation amount of the modulation algorithm.

7.1 Overview of Multilevel Inverter

The earliest multilevel inverter is the diode-clamped three-level inverter proposed by Nabae et al. [1], then various kinds of multilevel inverter appeared [2, 3]. The multilevel inverter is usually composed of several switching devices and capacitors, in which the capacitor voltages are superimposed by the control of the switches to form a multilevel staircase waveform. The three-level and *n*-level voltage control principle of one inverter bridge arm is shown in Fig. 7.1. It can be found that increasing the number of levels will result in an increase in the number of switching devices and capacitors, which makes the switching control more complicated.

The basic types of multilevel inverters include diode-clamped multilevel inverters, flying-capacitor multilevel inverters, and cascaded-bridge multilevel inverters. As shown in Fig. 7.2a, the DC link voltage of the diode-clamped multilevel inverter is divided to multiple levels by a group of series capacitors, while in the flying-capacitor multilevel inverter, the multiple levels are formed by capacitor ladder connections of different voltage levels as shown in Fig. 7.2b. However, the cascaded inverter is

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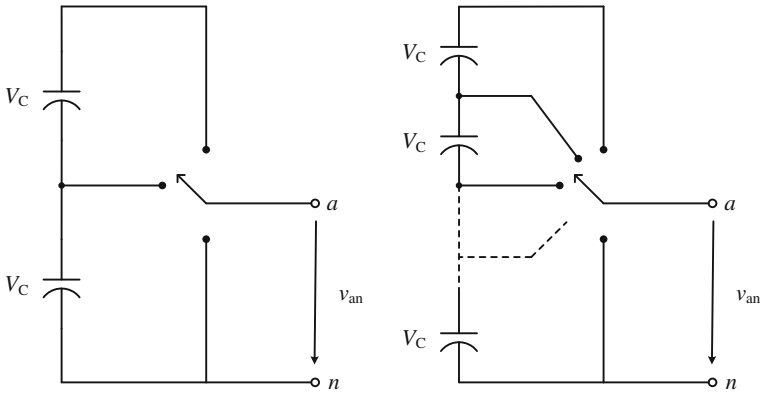
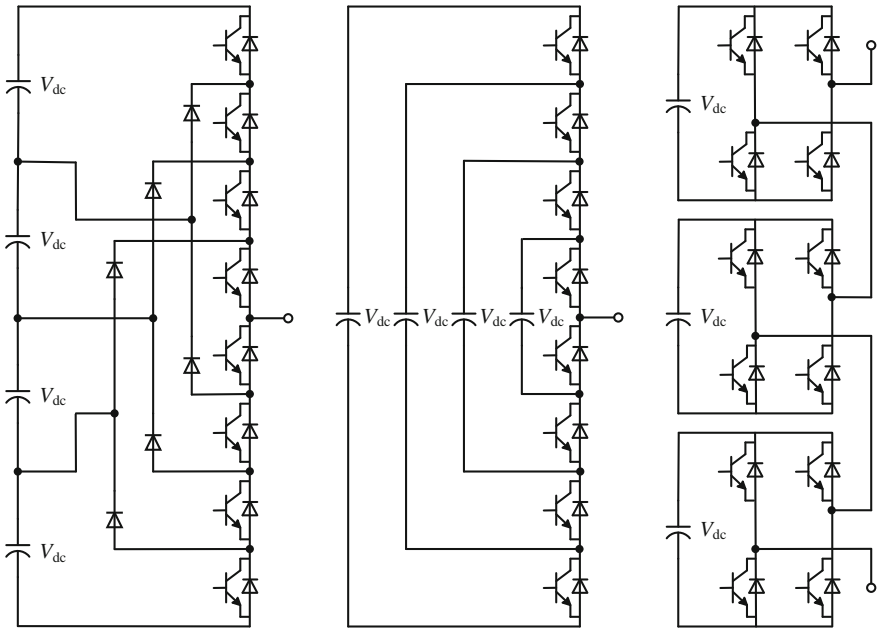


(a) Three-level. **(b)** *n*-level.

Fig. 7.1 Principle of single-phase multilevel inverter



(a) Diode-clamped. (b) Flying-capacitor. (c) Cascaded-bridge.

Fig. 7.2 Bridge arm structure of different types of multilevel inverters

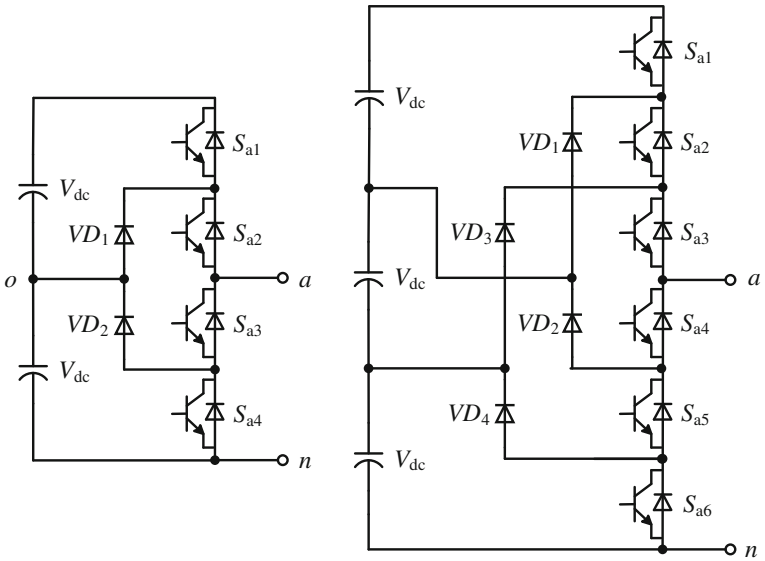
completely different, as shown in Fig. 7.2c, the outputs of a group of single-phase bridge inverters are connected in series to produce multiple levels.

7.1.1 Diode-Clamped Multilevel Inverter

According to the output level requirements of the inverter, the inverter topology of various levels can be obtained by the basic diode-clamped three-level inverter. For example, the bridge arm structures of the diode-clamped three-level and four-level inverters are given in Fig. 7.3.

Based on Fig. 7.3a, the switching states and the corresponding output voltages of the diode-clamped three-level inverter are listed in Table 7.1. It can be seen that the phase voltage v_{ao} can output $+V_{dc}$, 0 and $-V_{dc}$, so the line voltage has five levels, which are $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$. In the diode-clamped four-level inverter shown in Fig. 7.3b, the voltage v_{an} has four different outputs, which include $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$ and 0, then the line voltage can obtain six levels.

For a diode-clamped multilevel inverter, regardless of the number of levels, the blocking voltage of the main switching device is limited to V_{dc}, thus IGBT with low power consumption and low voltage level can be used in the high voltage occasions. However, the reverse voltage of the diode is $(k-2)V_{dc}$, where k is the number of



(a) Three-level. **(b)** Four-level.

Fig. 7.3 Bridge arm structure of the diode-clamped inverters

Table 7.1 Switching states and corresponding output voltages of the diode-clamped three-level inverter

State	v_{ao}	Switch ON	Switch OFF
1	V_{dc}	S_{a1} and S_{a2}	S_{a3} and S_{a4}
2	0	S_{a2} and S_{a3}	S_{a1} and S_{a4}
3	$-V_{dc}$	S_{a3} and S_{a4}	S_{a1} and S_{a2}

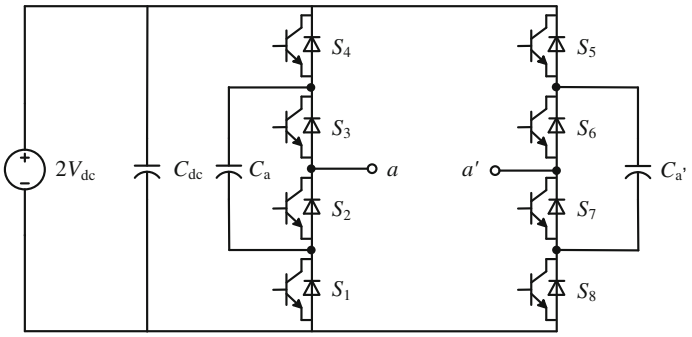


Fig. 7.4 Single-phase flying-capacitor three-level inverter

Table 7.2 Switching states and corresponding output voltages of the single-phase flying-capacitor three-level inverter

State	$v_{aa'}$	Switch ON
1	$-2V_{dc}$	S_1, S_2, S_5, S_6
2	$-V_{dc}$	S_1, S_3, S_5, S_6 or S_1, S_2, S_6, S_8
3	0	S_3, S_4, S_5, S_6, or S_1, S_2, S_7, S_8, or S_1, S_3, S_6, S_8
4	V_{dc}	S_3, S_4, S_6, S_8, or S_1, S_3, S_7, S_8
5	$2V_{dc}$	S_3, S_4, S_7, S_8

levels and $k \geq 3$; therefore, it is not practical for an inverter with an output level greater than 5.

7.1.2 Flying-Capacitor Multilevel Inverter

The single-phase flying-capacitor three-level inverter is illustrated in Fig. 7.4, and its switching states and corresponding output voltages are summarized in Table 7.2 [4]. It can be seen from Table 7.2 that the output voltage $v_{aa'} = 2V_{dc}$ when the switching devices S_3, S_4, S_7, and S_8 are turned on, while the output voltage $v_{aa'} = -2V_{dc}$ when S_1, S_2, S_5, and S_6 are turned on. Similarly, other output levels $+V_{dc}$, 0 and $-V_{dc}$ can be obtained by the device conduction laws in Table 7.2.

Compared with the diode-clamped multilevel inverters, the flying-capacitor multilevel inverters have the following problems: (1) the voltages on the capacitors are not equal, and the control of capacitor voltage is more difficult than the diode-clamp type; (2) the voltage of each capacitor is high, and the capacitance rating is generally larger than that of the diode-clamped multilevel inverter.

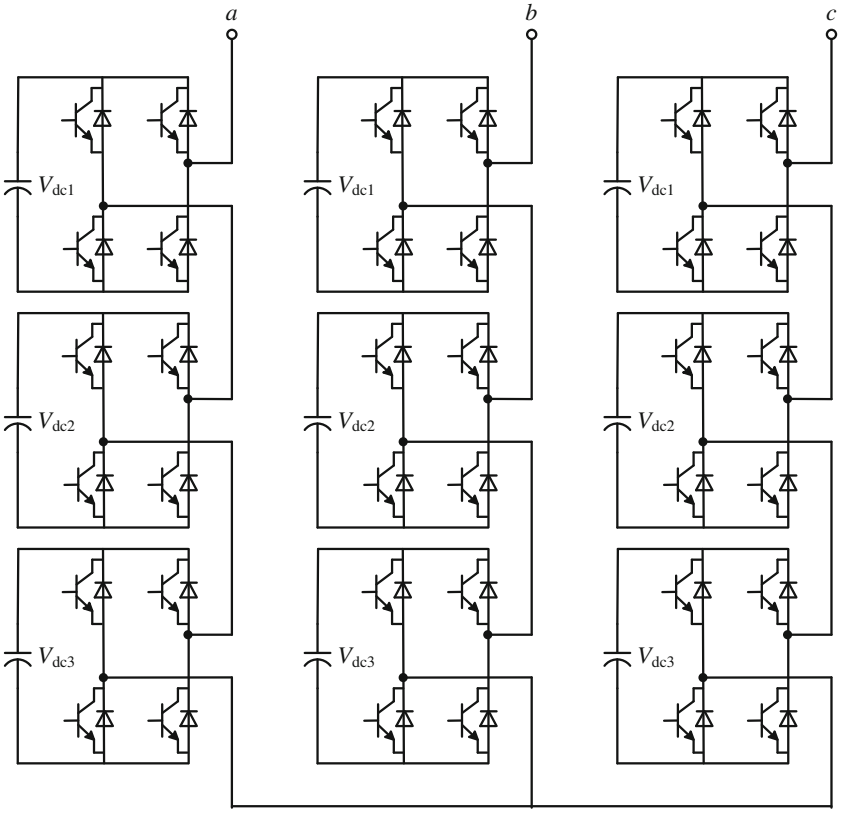


Fig. 7.5 Three-phase cascaded-bridge seven-level inverter

7.1.3 Cascaded-Bridge Multilevel Inverter

The three-phase cascaded-bridge seven-level inverter is shown in Fig. 7.5, in which each phase consists of three single-phase full-bridge inverter modules. As each full-bridge module can generate $+V_{dc}$, 0 and $-V_{dc}$, there are seven levels for each phase output. Therefore, for a multilevel inverter composed of N single-phase full-bridge modules cascaded per phase, $(2N + 1)$ output levels can be generated.

In the cascaded-bridge multilevel inverter, each single-phase full-bridge module needs an independent DC power supply, so the capacitor voltage is easy to be controlled, and the control of each single-phase full-bridge module can be independent. However, in order to coordinate control of each module, the control signals between the modules need communications. In general, the control of the cascaded-bridge multilevel inverters is simpler than that of the diode-clamped types and the flying-capacitor types.

7.2 Conventional SVPWM for Diode-Clamped Three-Level Inverter

The most commonly used diode-clamped three-level inverter is illustrated in Fig. 7.6, whose phase output is connected to the load via an LC filter.

The operating modes and the corresponding voltage space vectors of the diode-clamped three-level inverter under conventional SVPWM are listed in Table 7.3 [5–7]. Among the switch vectors, switch vector "2" corresponds to state 1 in Table 7.1, and the phase output voltage of the bridge arm is $v_{xo} = \frac{V_{dc}}{2}$, where $x = a, b, c$; switch vector "1" corresponds to state 2, and $v_{xo} = 0$; switch vector "0" corresponds to state 3, and $v_{xo} = -\frac{V_{dc}}{2}$. According to Table 7.3, there are 27 voltage space vectors corresponding to 27 operating modes, including 12 small vectors, six medium vectors, six large vectors, and three zero vectors. The distribution of all voltage vectors on the complex plane is shown in Fig. 7.7.

Unlike the two-level inverter which has only one kind of nonzero voltage vector, the output voltage vector of the diode-clamped three-level inverter can be composed of three kinds of vectors of different magnitudes, that is the large vector, the medium vector, and the small vector. The used vectors depend on the sector to which the reference voltage vector belongs.

As shown in Fig. 7.7, the complex plane can be divided into large sectors and small sectors by the voltage space vectors of the diode-clamped three-level inverter. The traditional six sectors, I, II, III, IV, V, and VI, can be considered as the large sectors,

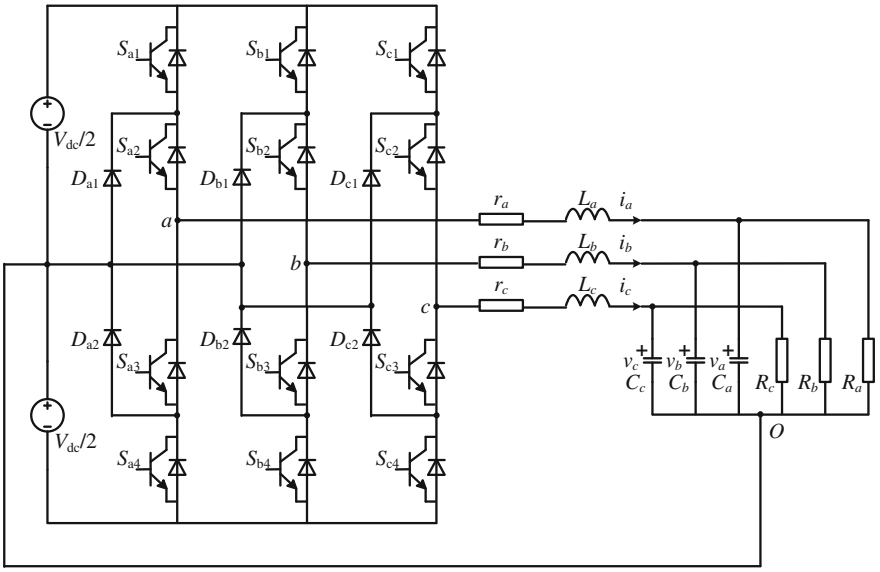


Fig. 7.6 Three-phase diode-clamped three-level inverter

Table 7.3 Operating modes and corresponding voltage vectors of the three-phase diode-clamped three-level inverter

Mode	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{c1}	S_{c2}	S_{c3}	S_{c4}	Switch vector	Voltage vector
1	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	100	$\vec{V}_{s1}$
2	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	110	$\vec{V}_{s2}$
3	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON	010	$\vec{V}_{s3}$
4	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	011	$\vec{V}_{s4}$
5	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	001	$\vec{V}_{s5}$
6	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	101	$\vec{V}_{s6}$
7	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	211	$\vec{V}_{s7}$
8	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	221	$\vec{V}_{s8}$
9	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	121	$\vec{V}_{s9}$
10	OFF	ON	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	122	$\vec{V}_{s10}$
11	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	112	$\vec{V}_{s11}$
12	ON	ON	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	OFF	212	$\vec{V}_{s12}$
13	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	ON	210	$\vec{V}_{s13}$
14	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	120	$\vec{V}_{s14}$
15	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	ON	ON	OFF	021	$\vec{V}_{s15}$

(continued)

Table 7.3 (continued)

Mode	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{b1}	S_{b2}	S_{b3}	S_{b4}	S_{c1}	S_{c2}	S_{c3}	S_{c4}	Switch vector	Voltage vector
16	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON	ON	OFF	OFF	012	$\vec{V}_{s16}$
17	OFF	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	102	$\vec{V}_{s17}$
18	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	201	$\vec{V}_{s18}$
19	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	ON	200	$\vec{V}_{s19}$
20	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	220	$\vec{V}_{s20}$
21	OFF	OFF	ON	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON	020	$\vec{V}_{s21}$
22	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	ON	OFF	OFF	022	$\vec{V}_{s22}$
23	OFF	OFF	ON	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF	002	$\vec{V}_{s23}$
24	ON	ON	OFF	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	202	$\vec{V}_{s24}$
25	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	222	$\vec{V}_{s25}$
26	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	111	$\vec{V}_{s26}$
27	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	000	$\vec{V}_{s27}$

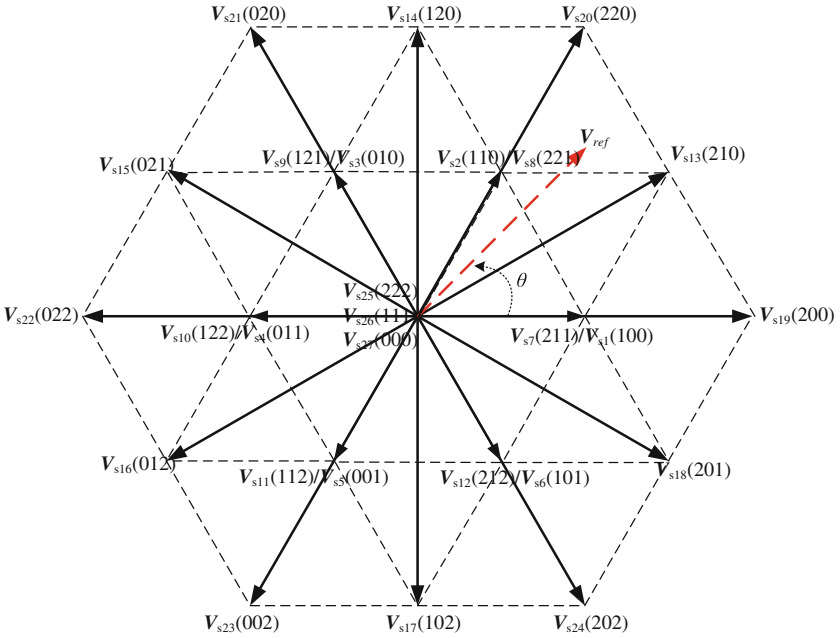


Fig. 7.7 Distribution of voltage space vectors of the three-phase diode-clamped three-level inverter

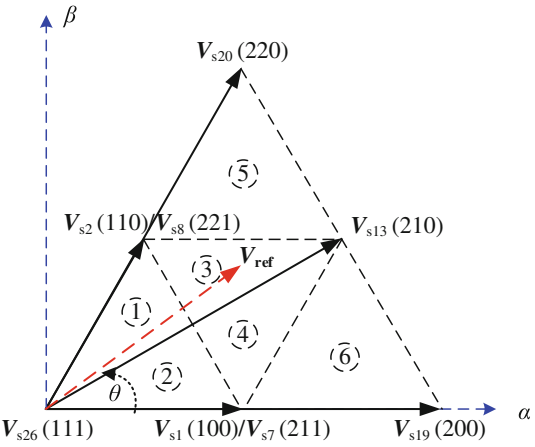


Fig. 7.8 Distribution of small sectors in large sector I

and each large sector can be further divided into six small sectors. The distribution of small sectors in large sector I is illustrated in Fig. 7.8.

To determine which specific small sector of a large sector the reference voltage $\vec{V}_{\text{ref}}$ is located in, the following equations can be used in accompany with $|V_{\text{ref}}|$ and θ. The criterion of small sectors has been summarized in Table 7.4. Assuming that

Table 7.4 Criterions of small sectors under conventional SVPWM

Small sector	Equation (7.2)	Equation (7.3)	Equation (7.4)	Equation (7.5)
①	True	–	–	True
②	True	–	–	False
③	False	False	False	True
④	False	False	False	False
⑤	False	–	True	–
⑥	False	True	–	–

$$\theta' = \theta - (k-1)\frac{\pi}{3} \tag{7.1}$$

where $k = 1, 2, 3, 4, 5, 6$ indicates the large sector in which the reference voltage locates.

$$|V_{\text{ref}}|\left(\cos\theta' + \frac{\sqrt{3}}{3}\sin\theta'\right) \le \frac{V_{\text{dc}}}{3} \tag{7.2}$$

$$|V_{\text{ref}}|\left(\cos\theta' - \frac{\sqrt{3}}{3}\sin\theta'\right) \ge \frac{V_{\text{dc}}}{3} \tag{7.3}$$

$$|V_{\text{ref}}|\sin\theta' \ge \frac{\sqrt{3}}{6}V_{\text{dc}} \tag{7.4}$$

$$\theta' \ge \pi/6 \tag{7.5}$$

The following two conditions must be observed to reduce the switching loss, when synthesizing the reference voltage vector by basic voltage vectors.

Condition 1: Only one switch is switched during state transition, which means that the transition from switch vector "0" to switch vector "2" and vice versa is not allowed.

Condition 2: The final state of present switching cycle will be the same as the initial state of the next switching cycle.

Considering the above switching conditions of the diode-clamped three-level inverter, the seven-segment switching sequences for each sector are listed in Table 7.5. Since the diode-clamped three-level inverter has redundant vectors, for example, small vectors 100 and 211 have the same magnitude and phase angle, the selection of the switching sequence has a large degree of freedom, and Table 7.5 only provides a conventional SVPWM method selected in this chapter.

Table 7.5 Switching sequences of conventional SVPWM

Large sector	Small sector	Switching sequence
I	①	110-111-211-221-211-111-110
	②	100-110-111-211-111-110-100
	③	110-210-211-221-211-210-110
	④	100-110-210-211-210-110-100
	⑤	110-210-220-221-220-210-110
	⑥	100-200-210-211-210-200-100
II	①	121-111-110-010-110-111-121
	②	110-111-121-221-121-111-110
	③	010-110-120-121-120-110-010
	④	110-120-210-211-210-110-100
	⑤	010-020-120-121-120-020-010
	⑥	110-120-220-221-220-120-110
III	①	010-011-111-121-111-011-010
	②	011-111-121-122-121-111-011
	③	011-021-121-122-121-021-011
	④	010-011-021-121-021-011-010
	⑤	011-021-022-122-022-021-011
	⑥	010-020-021-121-021-020-020
IV	①	011-111-112-122-112-111-011
	②	001-011-111-112-111-011-001
	③	001-011-012-112-012-011-001
	④	011-012-112-122-112-012-011
	⑤	001-002-012-112-012-002-001
	⑥	011-012-022-122-022-012-011
V	①	001-101-111-112-111-101-001
	②	101-111-112-212-112-111-101
	③	101-102-112-212-112-102-101
	④	001-101-102-112-102-101-001
	⑤	101-102-202-212-202-102-101
	⑥	001-002-102-112-102-002-001
VI	①	101-111-211-212-211-111-101
	②	100-101-111-211-111-101-100
	③	100-101-201-211-201-101-100
	④	101-201-211-212-211-201-101
	⑤	100-200-201-211-201-200-100
	⑥	101-201-202-212-202-201-101

7.3 m-Mode SVPWM for Diode-Clamped Three-Level Inverter

7.3.1 Switched Linear System Model

For the diode-clamped three-level inverter shown in Fig. 7.6, the currents flowing through the filter inductors i_a, i_b, i_c, and the voltages across the filter capacitors v_a, v_b, v_c are selected as the state variables, that is, $x = [i_a, i_b, i_c, v_a, v_b, v_c]^{\mathrm{T}}$. For the sake of analysis, it is assumed that the capacitance of all capacitors, the inductance of all inductors, and the resistance of all resistors are equal, that is, $C_a = C_b = C_c = C$, $L_a = L_b = L_c = L$, $r_a = r_b = r_c = r$ and $R_a = R_b = R_c = R$. Therefore, the switched linear system model of the diode-clamped three-level inverter similar to Eq. (2.1) can be obtained, where

$$A_1 = \cdots = A_{27} = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} & 0 \\ 0 & 0 & -\frac{r}{L} & 0 & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} & 0 \\ 0 & 0 & \frac{1}{C} & 0 & 0 & -\frac{1}{RC} \end{bmatrix} \tag{7.6}$$

$$B_1 = \left[0\ -\tfrac{1}{2L}\ -\tfrac{1}{2L}\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.7}$$

$$B_2 = \left[0\ 0\ -\tfrac{1}{2L}\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.8}$$

$$B_3 = \left[-\tfrac{1}{2L}\ 0\ -\tfrac{1}{2L}\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.9}$$

$$B_4 = \left[-\tfrac{1}{2L}\ 0\ 0\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.10}$$

$$B_5 = \left[-\tfrac{1}{2L}\ -\tfrac{1}{2L}\ 0\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.11}$$

$$B_6 = \left[0\ -\tfrac{1}{2L}\ 0\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.12}$$

$$B_7 = \left[\tfrac{1}{2L}\ 0\ 0\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.13}$$

$$B_8 = \left[\tfrac{1}{2L}\ \tfrac{1}{2L}\ 0\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.14}$$

$$B_9 = \left[0\ \tfrac{1}{2L}\ 0\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.15}$$

$$B_{10} = \left[0\ \tfrac{1}{2L}\ \tfrac{1}{2L}\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.16}$$

$$B_{11} = \left[0\ 0\ \tfrac{1}{2L}\ 0\ 0\ 0\right]^{\mathrm{T}} \tag{7.17}$$

$$B_{12} = \left[\begin{array}{ccccc} \frac{1}{2L} & 0 & \frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.18}$$

$$B_{13} = \left[\begin{array}{ccccc} \frac{1}{2L} & 0 & -\frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.19}$$

$$B_{14} = \left[\begin{array}{ccccc} 0 & \frac{1}{2L} & -\frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.20}$$

$$B_{15} = \left[\begin{array}{ccccc} -\frac{1}{2L} & \frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.21}$$

$$B_{16} = \left[\begin{array}{ccccc} -\frac{1}{2L} & 0 & \frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.22}$$

$$B_{17} = \left[\begin{array}{ccccc} 0 & -\frac{1}{2L} & \frac{1}{2\mathrm{L}} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.23}$$

$$B_{18} = \left[\begin{array}{ccccc} \frac{1}{2L} & -\frac{1}{2L} & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.24}$$

$$B_{19} = \left[\begin{array}{ccccc} \frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.25}$$

$$B_{20} = \left[\begin{array}{ccccc} \frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.26}$$

$$B_{21} = \left[\begin{array}{ccccc} -\frac{1}{2L} & \frac{1}{2L} & -\frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.27}$$

$$B_{22} = \left[\begin{array}{ccccc} -\frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.28}$$

$$B_{23} = \left[\begin{array}{ccccc} -\frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.29}$$

$$B_{24} = \left[\begin{array}{ccccc} \frac{1}{2L} & -\frac{1}{2L} & \frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.30}$$

$$B_{25} = \left[\begin{array}{ccccc} \frac{1}{2L} & \frac{1}{2L} & \frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.31}$$

$$B_{26} = \left[\begin{array}{cccccc} 0 & 0 & 0 & 0 & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.32}$$

$$B_{27} = \left[\begin{array}{ccccc} -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} & 0 & 0 \end{array}\right]^{\mathrm{T}} \tag{7.33}$$

$$C_1 = \cdots = C_{27} = \left[\begin{array}{cccccc} 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \end{array}\right] \tag{7.34}$$

7.3.2 m-*Mode Controllability*

According to the Controllability Criterion 2.1 for power converters, the controllability analysis of the diode-clamped three-level inverter will be carried out in this section. Since the operating modes 25, 26, and 27 represent for the zero voltage vectors, the

number of effective operating modes is 24, and the matrix corresponding to Eq. (2.6) can be constructed as below [8].

$$\begin{aligned}&[B_1, \ldots, B_{24}, A_1B_1, \ldots, A_{24}B_1, \ldots, A_1B_{24}, \ldots, A_{24}B_{24},\\ &A_1^2B_1, \ldots, A_1A_{24}B_1, \ldots, A_1^2B_{24}, \ldots, A_1A_{24}B_{24}, \ldots,\\ &A_1^{23}B_1, \ldots, A_1^{22}A_{24}B_1, \ldots, A_{24}^{22}A_1B_{24}, \ldots, A_{24}^{23}B_{24}]\end{aligned} \tag{7.35}$$

That is,

$$[\widehat{B}, \widehat{A}_1, \widehat{A}_2, \ldots, \widehat{A}_{23}] \tag{7.36}$$

According to Eqs. (7.7)–(7.30), it is obvious that $\widehat{B} = [B_1, B_2 \ldots, B_{24}]$ is non-full rank, while $\widehat{A}_1 = [A_1\widehat{B}, A_2\widehat{B}, \ldots, A_{24}\widehat{B}]$ is a matrix of 6×24^{24} dimensions, and it is easy to calculate out that its rank equals the number of state variables, that is

$$\text{rank}[\widehat{A}_1] = p = 6 \tag{7.37}$$

which means that the diode-clamped three-level inverter is state controllable [9].

Based on Eq. (2.8), seven control variables can be generated when the number of operating modes $m = 3$ is selected, which is greater than the number of state variables of the inverter. Therefore, the minimum number of the operating modes of the diode-clamped three-level inverter is 3. Referring to the control strategies of the three-phase four-wire inverter in Chap. 3, three symmetric vectors or operating modes of the diode-clamped three-level inverter can be selected to form a new switching sequence. For example, the small vector combinations include $\sigma \in (1, 3, 5)$, $\sigma \in (2, 4, 6)$, $\sigma \in (7, 9, 11)$ and $\sigma \in (8, 10, 12)$; the medium vector combinations are $\sigma \in (13, 15, 17)$ and $\sigma \in (14, 16, 18)$; and the large vector combinations are $\sigma \in (19, 21, 23)$ and $\sigma \in (20, 22, 24)$. The corresponding voltage space vectors of the above vector combinations are shown in Fig. 7.9.

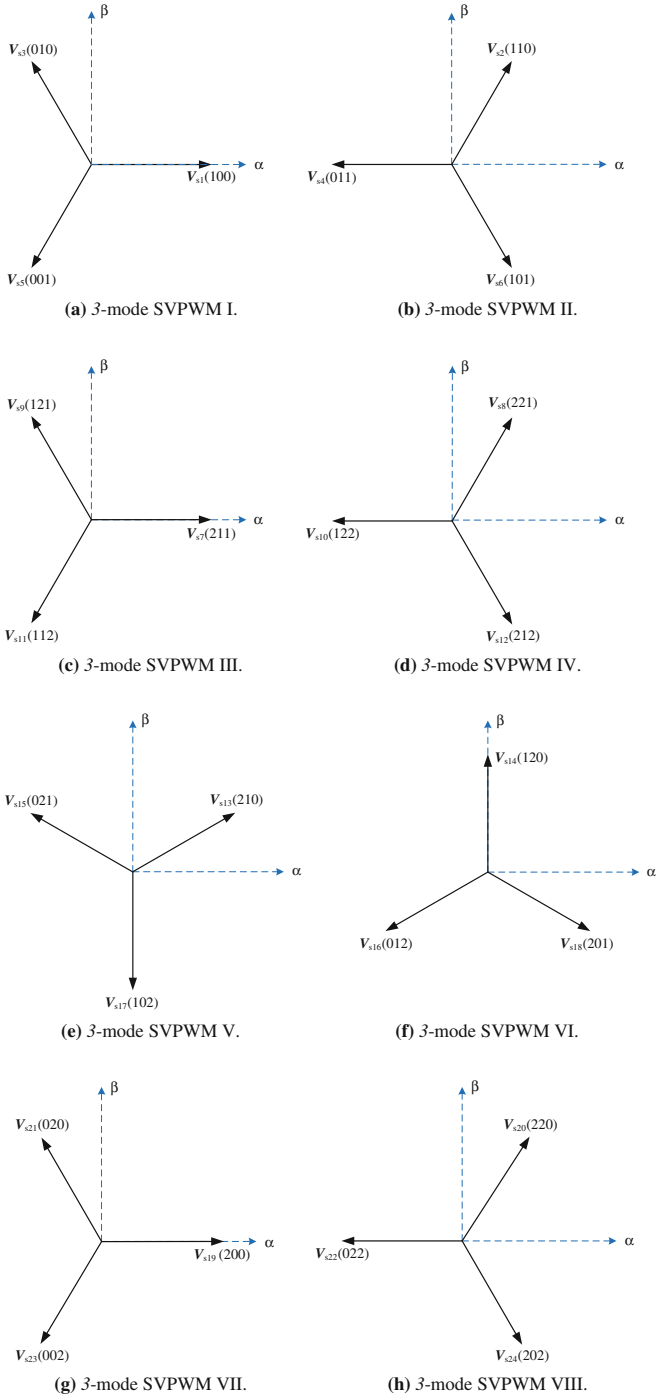
The ranks of the matrixes under the abovementioned switching sequences are calculated as follows, which prove that the diode-clamped three-level inverter is 3-mode controllable:

$$\begin{aligned}&\text{rank}[B_1, B_3, B_5, A_1B_1, A_3B_1, A_5B_1, A_1B_3,\\ &\quad A_3B_3, A_5B_3, A_1B_5, A_3B_5, A_5B_5] = 6\end{aligned} \tag{7.38}$$

$$\begin{aligned}&\text{rank}[B_2, B_4, B_6, A_2B_2, A_4B_2, A_6B_2, A_2B_4,\\ &\quad A_4B_4, A_6B_4, A_2B_6, A_4B_6, A_6B_6] = 6\end{aligned} \tag{7.39}$$

$$\begin{aligned}&\text{rank}[B_7, B_9, B_{11}, A_7B_7, A_9B_7, A_{11}B_7, A_7B_9,\\ &\quad A_9B_9, A_{11}B_9, A_7B_{11}, A_9B_{11}, A_{11}B_{11}] = 6\end{aligned} \tag{7.40}$$

$$\begin{aligned}&\text{rank}[B_8, B_{10}, B_{12}, A_8B_8, A_{10}B_8, A_{12}B_8, A_8B_{10},\\ &\quad A_{10}B_{10}, A_{12}B_{10}, A_8B_{12}, A_{10}B_{12}, A_{12}B_{12}] = 6\end{aligned} \tag{7.41}$$



(a) *3*-mode SVPWM I. **(b)** *3*-mode SVPWM II.

(c) *3*-mode SVPWM III. **(d)** *3*-mode SVPWM IV.

(e) *3*-mode SVPWM V. **(f)** *3*-mode SVPWM VI.

(g) *3*-mode SVPWM VII. **(h)** *3*-mode SVPWM VIII.

Fig. 7.9 Vector distributions of 3-mode SVPWMs

$$\begin{aligned}\operatorname{rank}[&B_{13}, B_{15}, B_{17}, A_{13}B_{13}, A_{15}B_{13}, A_{17}B_{13}, A_{13}B_{15},\\ &A_{15}B_{15}, A_{17}B_{15}, A_{13}B_{17}, A_{15}B_{17}, A_{17}B_{17}] = 6\end{aligned} \tag{7.42}$$

$$\begin{aligned}\operatorname{rank}[&B_{14}, B_{16}, B_{18}, A_{14}B_{14}, A_{16}B_{14}, A_{18}B_{14}, A_{14}B_{16},\\ &A_{16}B_{16}, A_{18}B_{16}, A_{14}B_{18}, A_{16}B_{18}, A_{18}B_{18}] = 6\end{aligned} \tag{7.43}$$

$$\begin{aligned}\operatorname{rank}[&B_{19}, B_{21}, B_{23}, A_{19}B_{19}, A_{21}B_{19}, A_{23}B_{19}, A_{19}B_{21},\\ &A_{21}B_{21}, A_{23}B_{21}, A_{19}B_{23}, A_{21}B_{23}, A_{23}B_{23}] = 6\end{aligned} \tag{7.44}$$

$$\begin{aligned}\operatorname{rank}[&B_{20}, B_{22}, B_{24}, A_{20}B_{20}, A_{22}B_{20}, A_{24}B_{20}, A_{20}B_{22},\\ &A_{22}B_{22}, A_{24}B_{22}, A_{20}B_{24}, A_{22}B_{24}, A_{24}B_{24}] = 6\end{aligned} \tag{7.45}$$

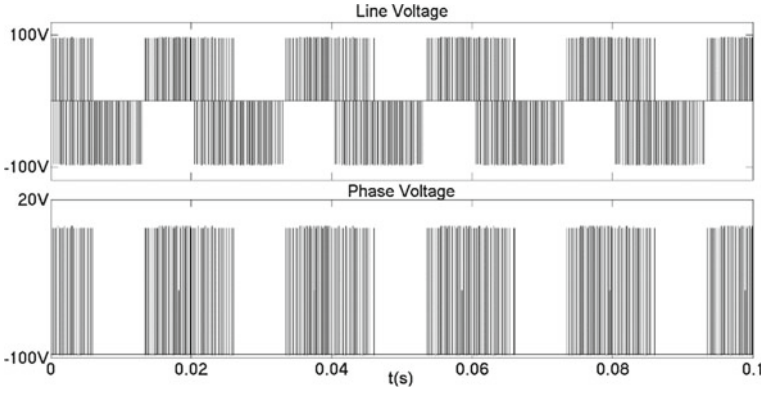
Since the three-level inverter requires the switching state of the bridge arm to switch between two adjacent states, that is, only the switching transitions between 0 and 1, or 1 and 2 are allowed, and there is no transition between 0 and 2. Therefore, it is necessary to insert a suitable zero voltage vector in the 3-mode SVPWM scheme to obtain a continuous switching sequence, although the above eight 3-mode SVPWM schemes can satisfy the controllability criterion. For example, by inserting a zero voltage vector 000 in the 3-mode SVPWM I, a continuous switching sequence like 100-000-010, 010-000-001, 001-000-100 can be obtained. However, in the 3-mode SVPWMs V–VIII shown in Fig. 7.9e–h, three bridge arms are all involved in each switching process at the same time, which will increase the number of switching times and the complexity of the control algorithm. As a result, 3-mode SVPWMs V–VIII are not recommended [9].

The 3-mode SVPWMs I–IV shown in Fig. 7.9a–d are used to verify their feasibility in the simulation, where the DC voltage V_{dc} is set to be 200 V, the fundamental frequency of output voltage is 50 Hz. The output line voltage and phase voltage waveforms are shown in Fig. 7.10. It can be seen that only three operating modes are needed to generate a sinusoidal line voltage waveform, which proves that the diode-clamped three-level inverter is complete state controllable by using only three nonzero voltage vectors.

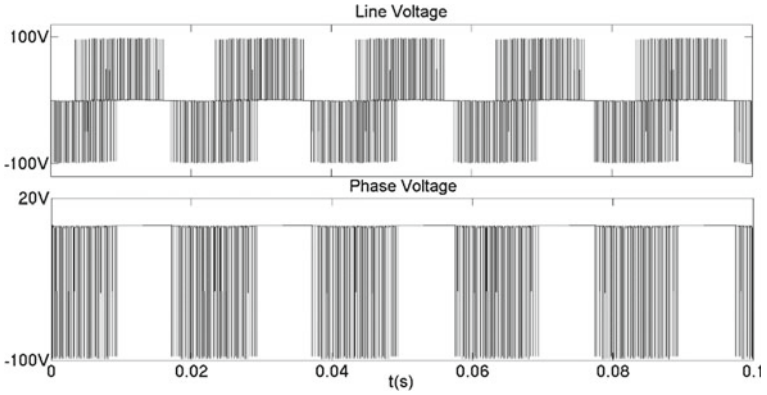
7.3.3 9-Mode SVPWM

According to the m-mode controllability definition, 3-mode SVPWM is only one of many m-mode SVPWMs for the diode-clamped three-level inverter, and it is the one containing least modes. However, since the 3-mode SVPWM only uses a single type of voltage vector, the output phase voltage contains only two levels without the characteristics of three levels. In order to achieve the multilevel output characteristics, it is necessary to adopt different types of voltage vector in the mode combination scheme, that is, to adopt different types of operating modes to construct SVPWM.

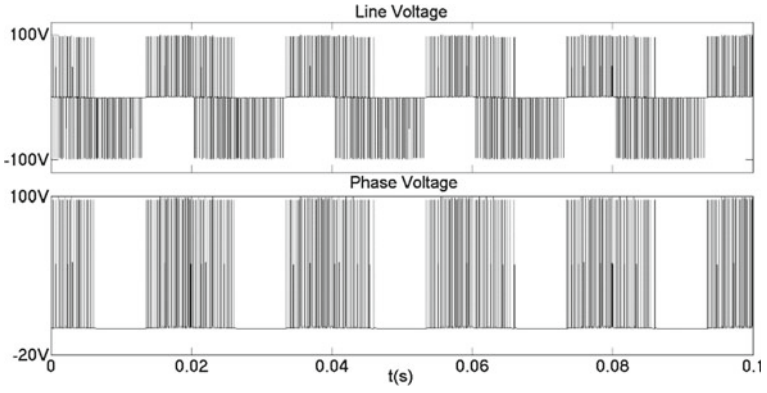
Considering the principle of producing three-level voltage and the switching conditions to minimize the number of switching times, the small vectors in Fig. 7.9a can be combined with the large vectors in Fig. 7.9g, or the small vectors in Fig. 7.9c



(a) *3*-mode SVPWM I.

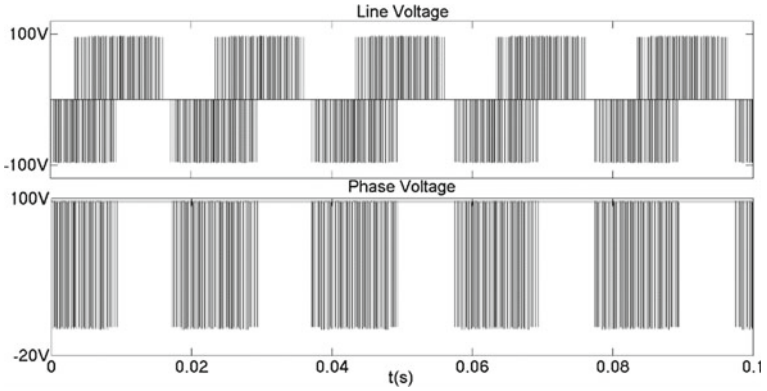


(b) *3*-mode SVPWM II.



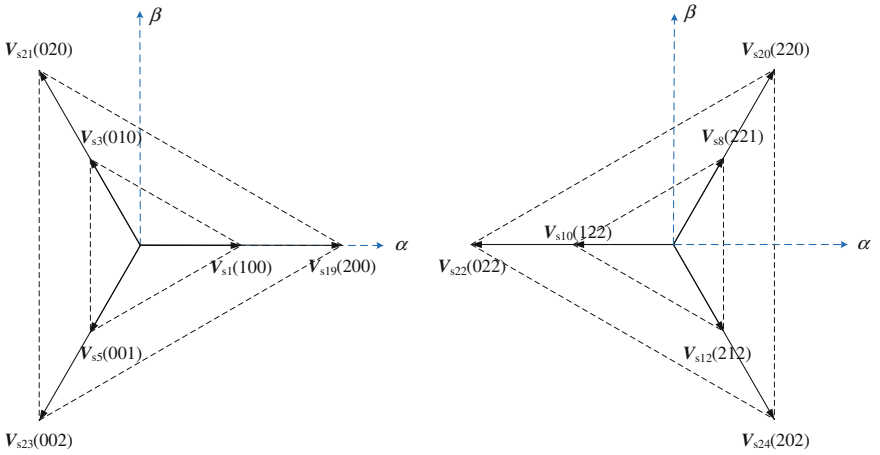
(c) *3*-mode SVPWM III.

Fig. 7.10 Simulation results of the diode-clamped three-level inverter with 3-mode SVPWMs



(d) *3*-mode SVPWM IV.

Fig. 7.10 (continued)



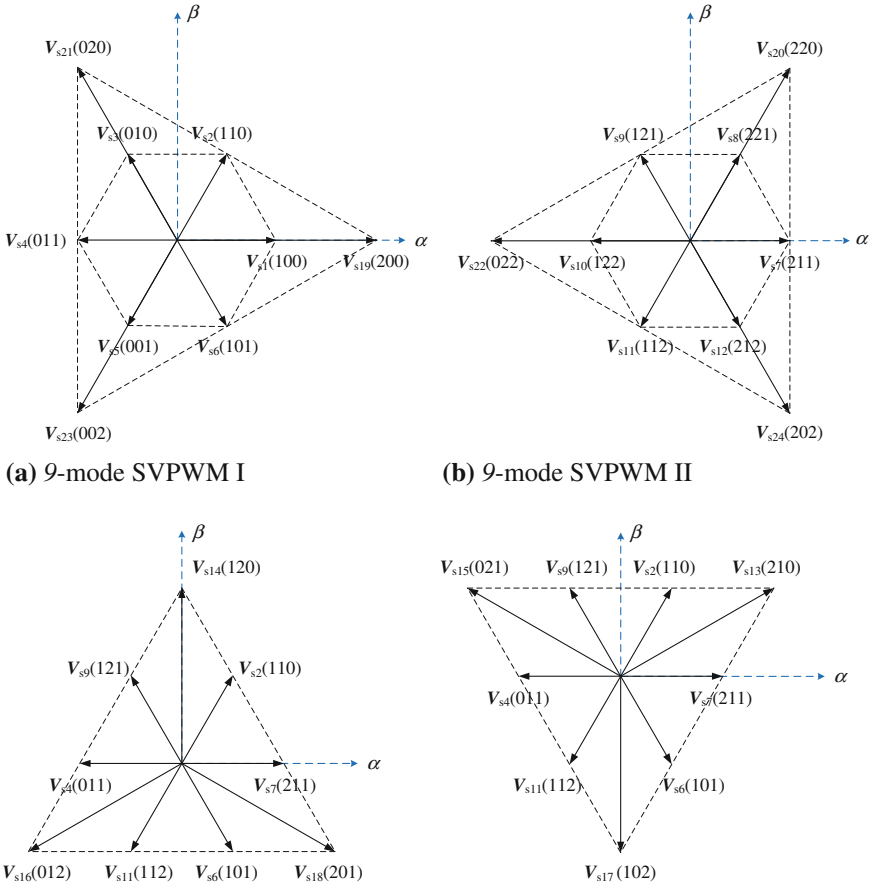
(a) *6*-mode SVPWM I. **(b)** *6*-mode SVPWM II.

Fig. 7.11 Vector distribution of typical 6-mode SVPWMs

combined with the large vectors in Fig. 7.9h, to obtain two kinds of 6-mode SVPWMs as shown in Fig. 7.11. The rank of the controllability matrix of diode-clamped three-level inverter under 6-mode SVPWM is calculated as below:

$$\text{rank}\left[B_1, B_3, B_5, B_{19}, B_{21}, B_{23}, A_1B_1, \ldots, A_{23}B_1, A_1B_3, \ldots A_{23}B_3, \ldots, A_{23}B_{23}\right] = 6 \tag{7.46}$$

$$\text{rank}[B_8, B_{10}, B_{12}, B_{20}, B_{22}, B_{24}, A_8B_8, \ldots, A_{24}B_8, A_8B_{10}, \ldots A_{24}B_{10}, \ldots, A_{24}B_{24}] = 6 \tag{7.47}$$



(a) *9*-mode SVPWM I **(b)** *9*-mode SVPWM II

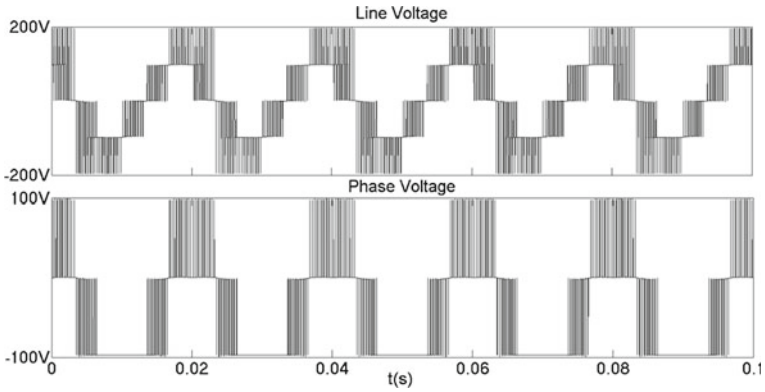
(c) *9*-mode SVPWM III. **(d)** *9*-mode SVPWM IV.

Fig. 7.12 Vector distribution of 9-mode SVPWMs

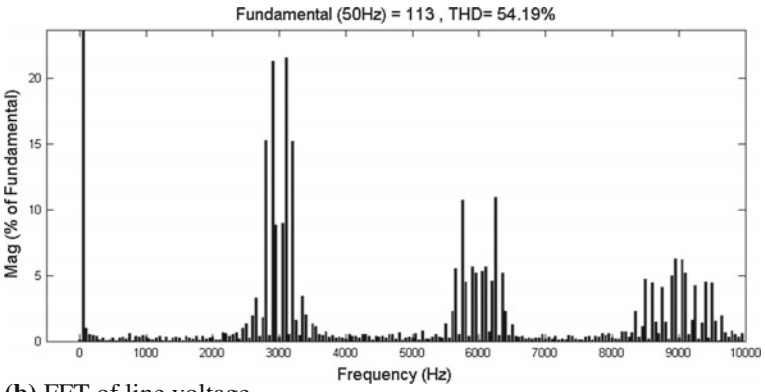
Therefore, the diode-clamped three-level inverter is 6-mode controllable.

In the 6-mode SVPWM schemes shown in Fig. 7.11, the complex plane is divided into three large sectors, similar to the 3-mode SVPWM of three-phase four-wire inverter, the current imbalance problem between upper and lower arms is inevitable. Therefore, three small vectors of different phases can be added to the 6-mode SVPWM, then two kinds of 9-mode SVPWM can be obtained, which are shown in Fig. 7.12a, b.

Both 9-mode SVPWM I and 9-mode SVPWM II are the combinations of six small vectors and three large vectors. In fact, the combination of six small vectors and three medium vectors can also satisfy the three-level output characteristics. Under the premise of reducing the number of switching times when synthesizing the voltage vector, the other two kinds of 9-mode SVPWMs are shown in Fig. 7.12c, d.



(a) Line voltage and phase voltage.



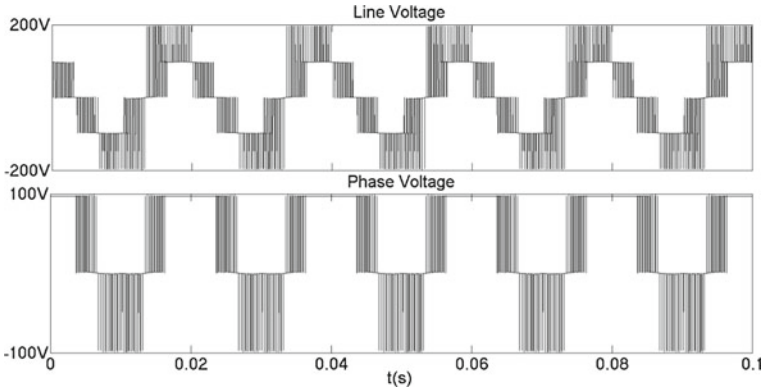
(b) FFT of line voltage.

Fig. 7.13 Simulation results of the diode-clamped three-level inverter with 9-mode SVPWM I

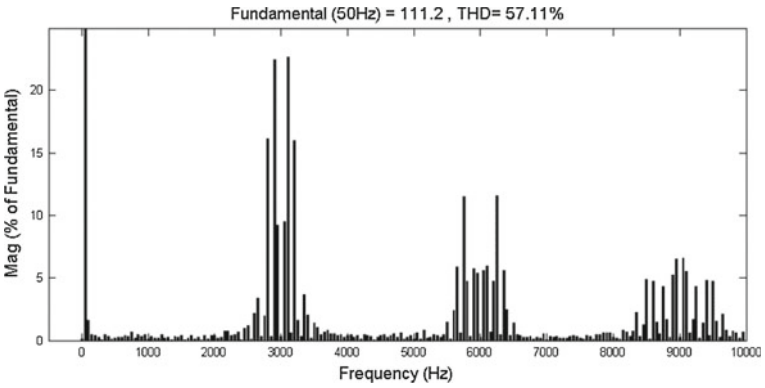
Simulation results by using the 9-mode SVPWMs are shown in Figs. 7.13, 7.14, 7.15 and 7.16. It can be seen that the three-level output of the phase voltage can be achieved, which satisfies the output requirements of the three-level inverter. However, due to the phenomenon that the output phase voltage is partially clamped, the line voltage waveform has an asymmetrical distortion and the harmonic content is relatively large.

7.3.4 12-*Mode SVPWM*

In order to solve the shortcomings of 9-mode SVPWM, the operating modes of the inverter can be further increased on the basis of 9-mode SVPWM, to supplement the missing modulation regions, and the modulation degree can be increased as a



(a) Line voltage and phase voltage.



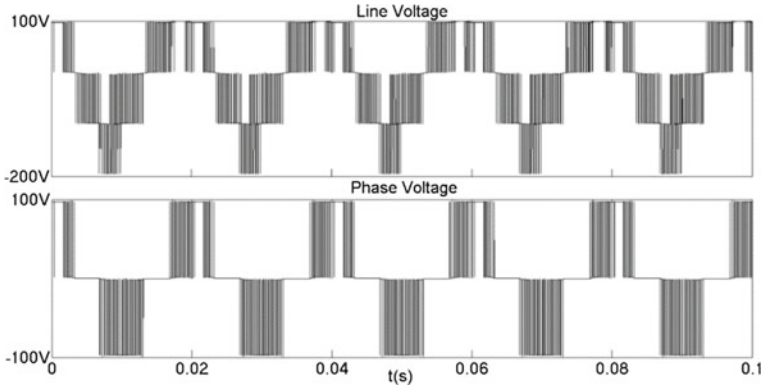
(b) FFT of line voltage.

Fig. 7.14 Simulation results of the diode-clamped three-level inverter with 9-mode SVPWM II

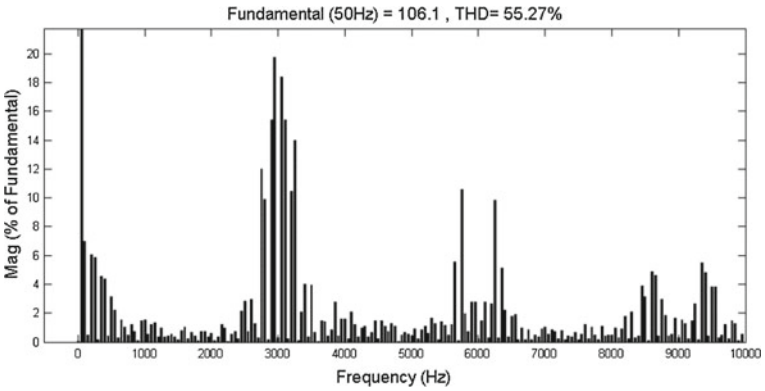
result. Since the phases of the medium vector and the small vector are inconsistent, six medium vectors and six small vectors can be selected and combined to make the basic voltage vector distribution on the complex plane more uniform. The vector distribution of 12-mode SVPWM is shown in Fig. 7.17, the 12 basic voltage vectors form a regular hexagonal modulation area, which is larger than the triangular modulation area of 9-mode SVPWMs.

The simulated waveform of the diode-clamped three-level inverter with 12-mode SVPWM is shown in Fig. 7.18.

Obviously, the phase voltage not only has three-level characteristics but also has high symmetry. In addition, the fundamental voltage content of the line voltage is higher than that of 9-mode SVPWMs, and the harmonic content is much lower than that of 9-mode SVPWMs, concentrated near the switching frequency. The low-order harmonic content is less, and the harmonics are easy to be filtered.



(a) Line voltage and phase voltage.



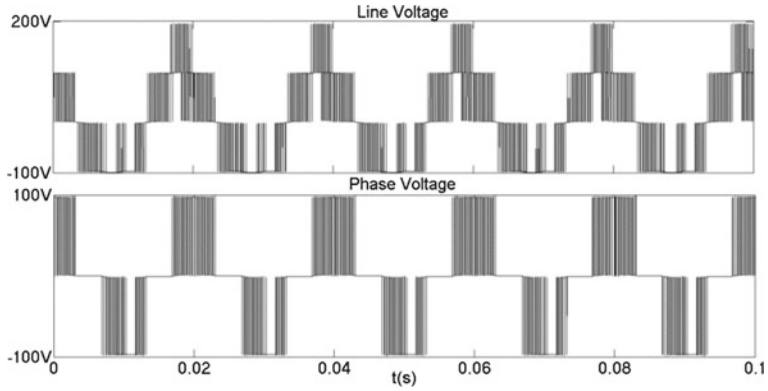
(b) FFT of line voltage.

Fig. 7.15 Simulation results of the diode-clamped three-level inverter with 9-mode SVPWM III

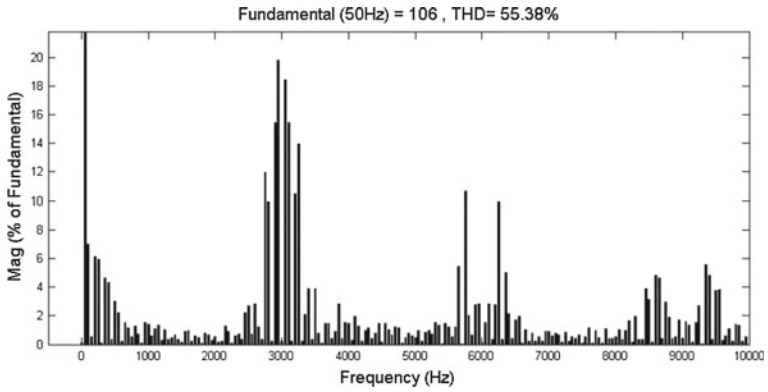
7.3.5 18-*Mode SVPWM*

Although the modulation ratio of 12-mode SVPWM is much higher than that of the 9-mode SVPWM, it is still lower than the conventional SVPWM. The reason is that the 12-mode SVPWM only uses the medium and small vectors. In order to further increase the modulation ratio to a level consistent with the conventional SVPWM, it is necessary to add large vectors to the current 12-mode SVPWM.

Therefore, an 18-mode SVPWM consists of six small vectors, six medium vectors, and six large vectors, which form three regular hexagons in the complex plane to obtain a modulation range similar to that of the conventional SVPWM. Since there are only six large vectors and six medium vectors, there is no redundant combination of large vectors and medium vectors. The type of 18-mode SVPWM depends on the combination of small vectors. Obviously, there are four combinations among 12 small



(a) Line voltage and phase voltage.



(b) FFT of line voltage.

Fig. 7.16 Simulation results of the diode-clamped three-level inverter with 9-mode SVPWM IV

vectors by considering their symmetry, and the corresponding vector distribution of 18-mode SVPWMs is shown in Fig. 7.19.

By analyzing the vector distribution of 18-mode SVPWM, it is found that the small sectors of 18-mode SVPWMs I and II are composed of continuous switching vectors, that is, only one phase signal differs between two adjacent voltage vectors, for example, the small vectors 211 and 221 as shown in Fig. 7.19a, and 100 and 110 in Fig. 7.19b. Therefore, two small vectors can be directly switched when synthesizing the voltage vector, and only one phase bridge arm is involved in the switching process. In the 18-mode SVPWM III shown in Fig. 7.19c, there are two different switching states between any two adjacent small vectors, such as small vectors 211 and 110. By inserting zero voltage vector 111, the switching times and voltage spikes of the switch can be effectively reduced. In the 18-mode SVPWM IV shown in Fig. 7.19d, there are three-phase signal different between the adjacent small vectors, such as

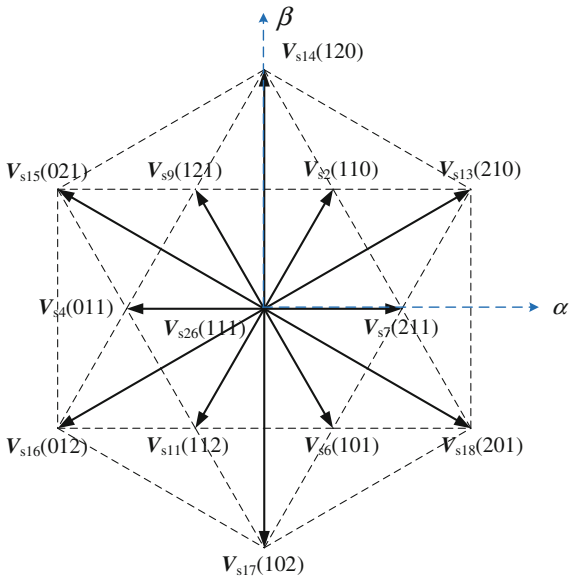


Fig. 7.17 Vector distribution of 12-mode SVPWM

small vectors 100 and 221, then two or three-phase bridge arms are involved in the switching process. As a result, 18-mode SVPWM IV scheme is not practical, because its number of switching times is significantly higher than that of the other three 18-mode SVPWMs.

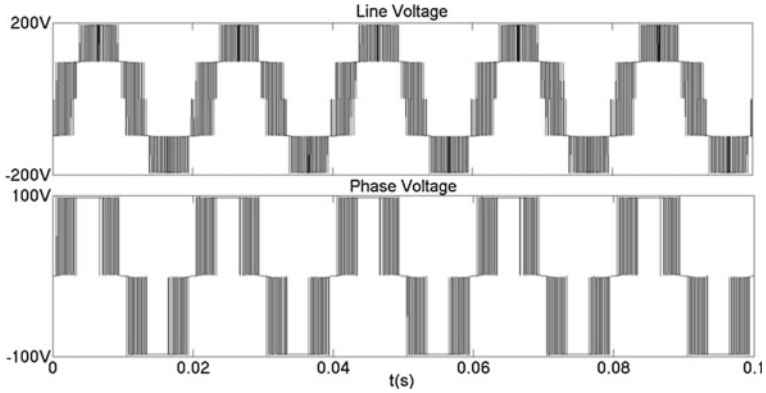
In the following parts, the 18-mode SVPWM I is taken as an example to illustrate how to synthesize the reference voltage vector. Since 18-mode SVPWM only adopts 18 nonzero voltage vectors, each large sector can only be divided into 4 equilateral triangle regions of the same equal size. The division method of the small regions in sector I is shown in Fig. 7.20, and the number of small sectors is reduced from six in the traditional SVPWM to four in 18-mode SVPWM.

The region in which the reference voltage vector locates is determined as follows. If Eq. (7.2) is established, then the reference vector locates in region R_1. If Eq. (7.3) is established, then the reference vector locates in region R_4. If neither of the above two equations is true, but Eq. (7.4) is established, then the reference vector locates in region R_3, otherwise in region R_2.

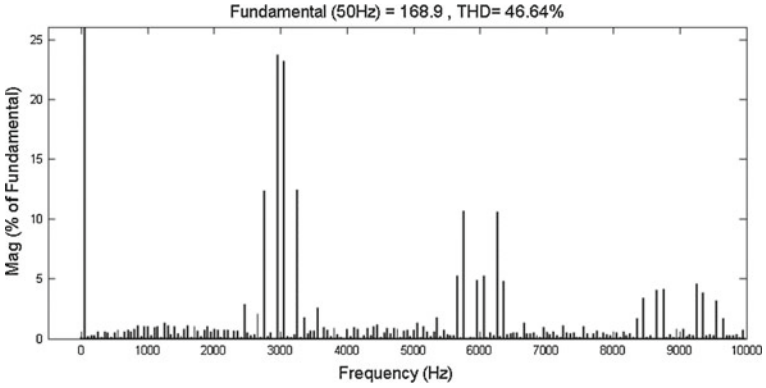
After the specific sector in which the reference voltage vector locates is known, the reference voltage vector can be synthesized by the three adjacent basic voltage vectors, $\vec{V}_x$, $\vec{V}_y$ and $\vec{V}_z$. According to the parallelogram rule, we have

$$\begin{cases} \vec{V}_{\text{ref}} \cdot T_s = \vec{V}_x \cdot T_x + \vec{V}_y \cdot T_y + \vec{V}_z \cdot T_z \\ T_s = T_x + T_y + T_z \end{cases} \tag{7.48}$$

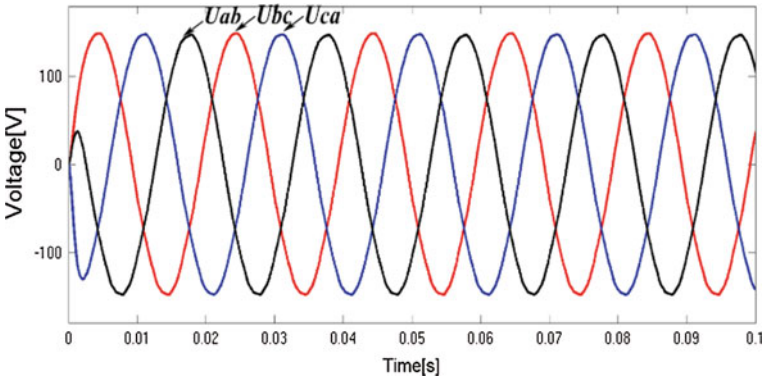
where T_x, T_y and T_z are the duration time of $\vec{V}_x$, $\vec{V}_y$ and $\vec{V}_z$, respectively.



(a) Line voltage and phase voltage.

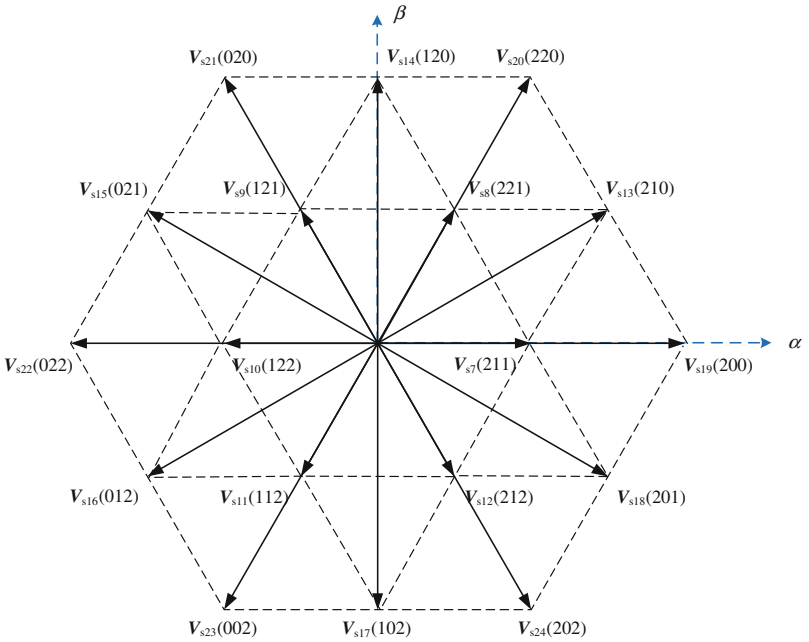


(b) FFT of line voltage.

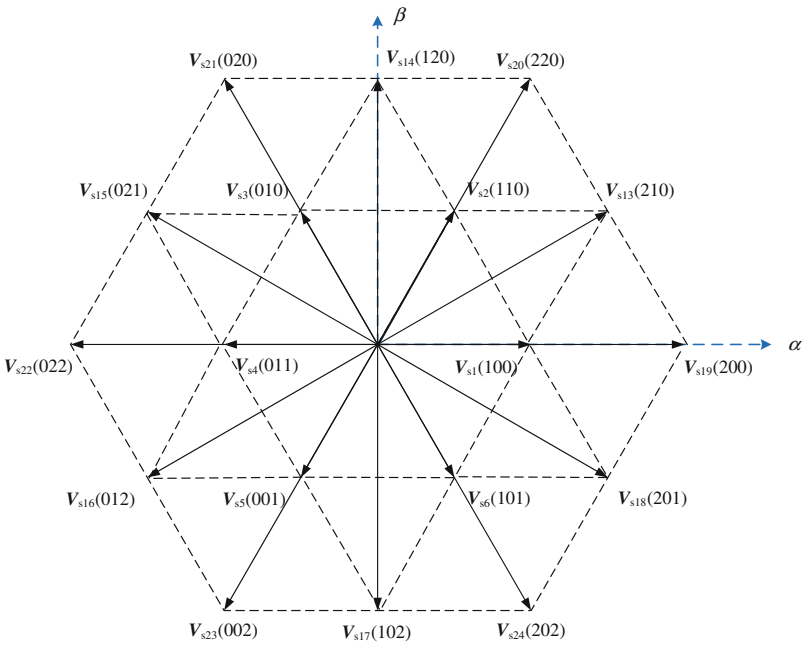


(c) Line voltages with filter.

Fig. 7.18 Simulation results of the diode-clamped three-level inverter with 12-mode SVPWM

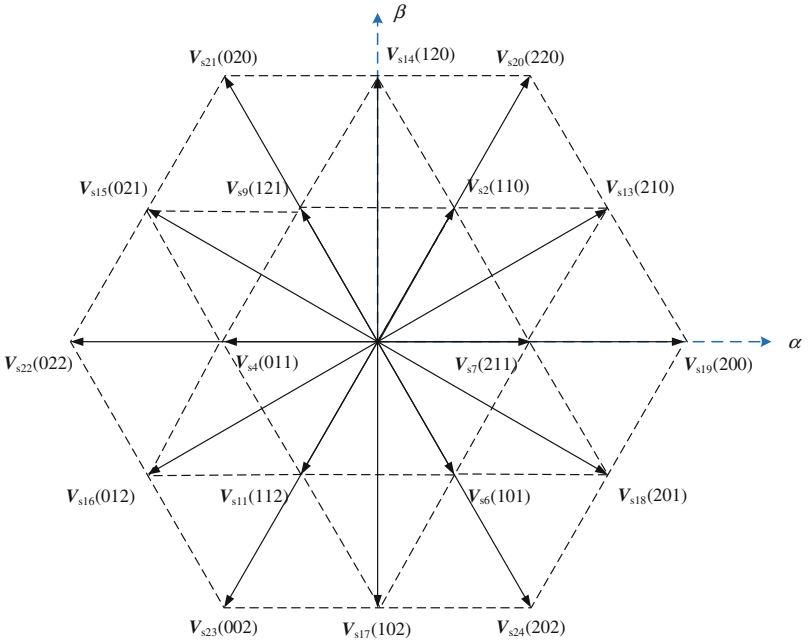


(a) *18*-mode SVPWM I

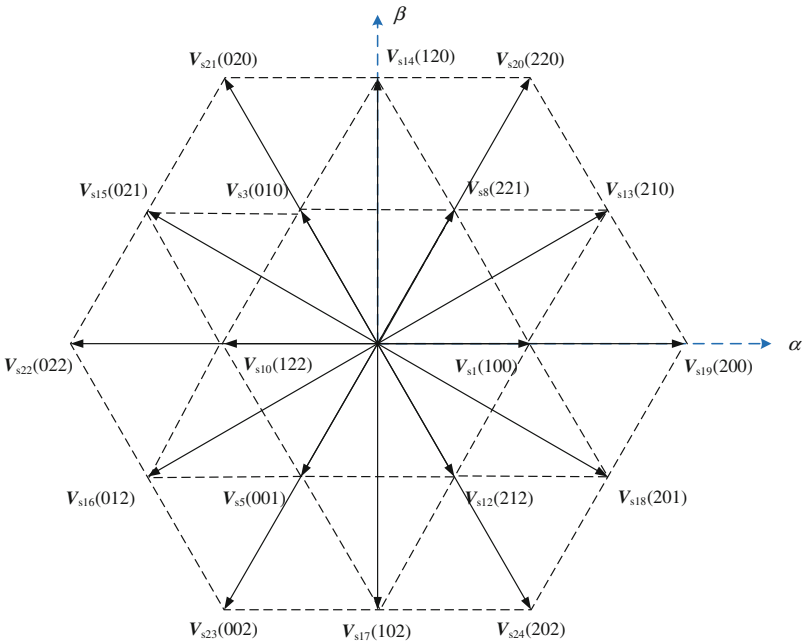


(b) *18*-mode SVPWM II.

Fig. 7.19 Vector distribution of 18-mode SVPWMs



(c) *18*-mode SVPWM III.



(d) *18*-mode SVPWM IV.

Fig. 7.19 (continued)

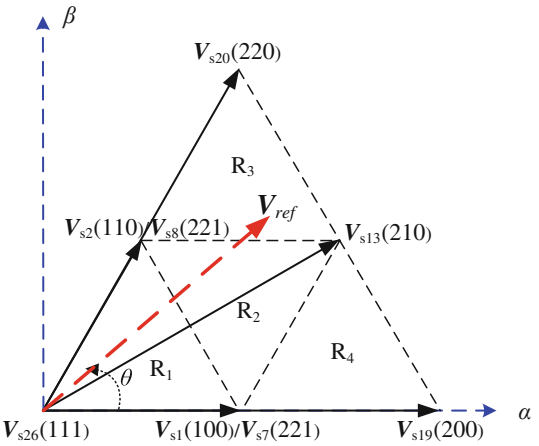


Fig. 7.20 Small region distribution of 18-mode SVPWM in large sector I

Unlike the two-level inverter, such as the three-phase four-wire inverter, the zero voltage vector is not necessary among the three basic voltage vectors which are required to form a reference voltage in Eq. (7.48). Taking the large sector I as an example, the switching sequences corresponding to four small regions are shown in Fig. 7.21.

Referring to the calculation method of vector duration time in the previous chapters, the duration time of each voltage vector in Fig. 7.21 can obtained by Eqs. (7.49)–(7.52). The duration time calculation in other sectors is basically the same.

$$\begin{cases} T_{s7} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(3\cos\theta - \sqrt{3}\sin\theta\right)\cdot T_s \\ T_{s8} = 2\sqrt{3}\frac{V_{\text{ref}}}{V_{\text{dc}}}\sin\theta\cdot T_s \\ T_{s26} = T_s - T_{s7} - T_{s8} \end{cases}, \quad \text{for Region R}_1 \tag{7.49}$$

$$\begin{cases} T_{s7} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(3\cos\theta + \sqrt{3}\sin\theta\right)\cdot T_s \\ T_{s8} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(-3\cos\theta + \sqrt{3}\sin\theta\right)\cdot T_s \\ T_{s13} = T_s - T_{s7} - T_{s8} \end{cases}, \quad \text{for Region R}_2 \tag{7.50}$$

$$\begin{cases} T_{s8} = \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(3\cos\theta + \sqrt{3}\sin\theta\right)\cdot T_s \\ T_{s13} = 2T_s - \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(3\cos\theta + 3\sqrt{3}\sin\theta\right)\cdot T_s \\ T_{s20} = T_s - T_{s8} - T_{s13} \end{cases}, \quad \text{for Region R}_3 \tag{7.51}$$

$$\begin{cases} T_{s7} = 2T_s - \frac{V_{\text{ref}}}{V_{\text{dc}}}\left(3\cos\theta + 3\sqrt{3}\sin\theta\right)\cdot T_s \\ T_{s13} = 2\sqrt{3}\frac{V_{\text{ref}}}{V_{\text{dc}}}\sin\theta\cdot T_s \\ T_{s19} = T_s - T_{s7} - T_{s13} \end{cases}, \quad \text{for Region R}_4 \tag{7.52}$$

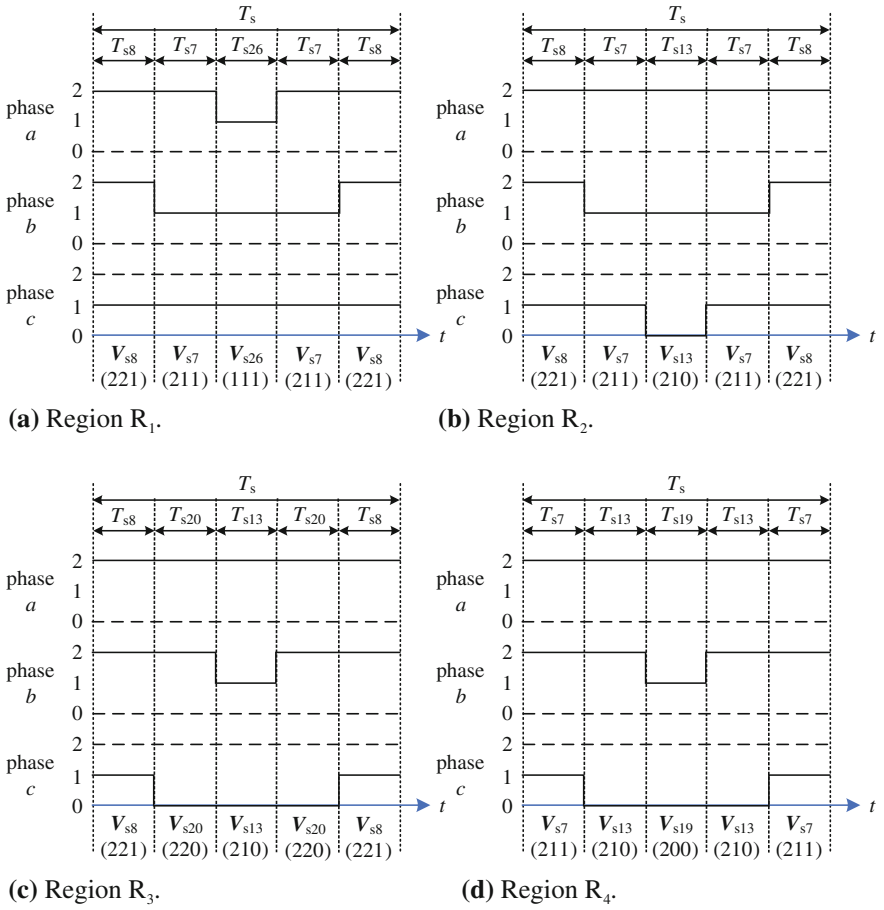


Fig. 7.21 Switching sequences of 18-mode SVPWM I in large sector I

In summary, when the 18-mode SVPWM I is applied to the diode-clamped three-level inverter, the corresponding switching sequences are listed in Table 7.6. Similarly, the switching sequences of 18-mode SVPWM II and III are given in Tables 7.7 and 7.8, respectively.

Simulation waveforms of output line voltage and phase voltage are shown in Figs. 7.22, 7.23 and 7.24, to verify the above three 18-mode SVPWMs of the diode-clamped three-level inverter. It is shown that when 18-mode SVPWMs I and II are used, the output phase voltage is positive–negative asymmetrical, and the midpoint potential is easy to shift. However, both the phase voltage and line voltage of 18-modes SVPWM III are positive–negative symmetrical, so it is more practical in applications.

Table 7.6 Switching sequences of 18-mode SVPWM I

Sector	Region	Switching sequences	Sector	Region	Switching sequences
I	R_1	221-211-111-211-221	IV	R_1	122-112-111-112-122
	R_2	221-211-210-211-221		R_2	122-112-012-112-122
	R_3	221-220-210-220-221		R_3	112-012-002-012-112
	R_4	211-210-200-210-211		R_4	122-022-012-022-122
II	R_1	221-121-111-121-221	V	R_1	212-112-111-112-212
	R_2	221-121-120-121-221		R_2	212-112-102-112-212
	R_3	121-120-020-120-121		R_3	212-202-102-202-212
	R_4	221-220-120-220-221		R_4	112-102-002-102-112
III	R_1	122-121-111-121-122	VI	R_1	212-211-111-211-212
	R_2	122-121-021-121-122		R_2	212-211-201-211-212
	R_3	122-022-021-022-122		R_3	211-201-200-201-211
	R_4	121-021-020-021-121		R_4	212-202-201-202-212

Table 7.7 Switching sequences of 18-mode SVPWM II

Sector	Region	Switching sequences	Sector	Region	Switching sequences
I	R_1	100-110-111-110-100	IV	R_1	001-011-111-011-001
	R_2	100-110-210-110-100		R_2	001-011-012-011-001
	R_3	110-210-220-210-110		R_3	001-002-012-002-001
	R_4	100-200-210-200-100		R_4	011-012-022-012-011
II	R_1	010-110-111-110-010	V	R_1	001-101-111-101-001
	R_2	010-110-120-110-010		R_2	001-101-102-101-001
	R_3	010-020-120-020-010		R_3	101-102-202-102-101
	R_4	110-120-220-120-110		R_4	001-002-102-002-001
III	R_1	010-011-111-011-010	VI	R_1	100-101-111-101-100
	R_2	010-011-021-011-010		R_2	100-101-201-101-100
	R_3	011-021-022-021-011		R_3	100-200-201-200-100
	R_4	010-020-021-020-010		R_4	101-201-202-201-101

7.4 Comparison of *m*-Mode SVPWM and Conventional SVPWM

In order to further understand the characteristics of the *m*-mode SVPWM, this section will compare several *m*-mode SVPWMs proposed in Sect. 7.3 with the conventional SVPWM in Sect. 7.2 comprehensively.

Table 7.8 Switching sequences of 18-mode SVPWM III

Sector	Region	Switching sequences	Sector	Region	Switching sequences
I	R_1	211-111-110-111-211	IV	R_1	011-111-112-111-011
	R_2	211-210-110-210-211		R_2	011-012-112-012-011
	R_3	110-210-220-210-110		R_3	112-012-002-012-112
	R_4	211-210-200-210-211		R_4	011-012-022-012-011
II	R_1	110-111-121-111-110	V	R_1	112-111-101-111-112
	R_2	110-120-121-120-110		R_2	112-102-101-102-112
	R_3	121-120-020-120-121		R_3	101-102-202-102-101
	R_4	110-120-220-120-110		R_4	112-102-002-102-112
III	R_1	121-111-011-111-121	VI	R_1	101-111-211-111-101
	R_2	121-021-011-021-121		R_2	101-201-211-201-101
	R_3	011-021-022-021-011		R_3	211-201-200-201-211
	R_4	121-021-020-021-121		R_4	101-201-201-201-101

7.4.1 DC Voltage Utilization

Since 9-mode SVPWMs I and II only use three large vectors and six small vectors, the maximum amplitude of reference voltage vector is $\frac{V_{dc}}{3}$. Correspondingly, the maximum modulation index of 9-mode SVPWMs I and II is

$$M = \frac{\pi V_{ref}}{2V_{dc}} = \frac{\pi \cdot \frac{1}{3} V_{dc}}{2V_{dc}} = \frac{\pi}{6}, \quad \text{for 9-mode SVPWMs I and II} \tag{7.53}$$

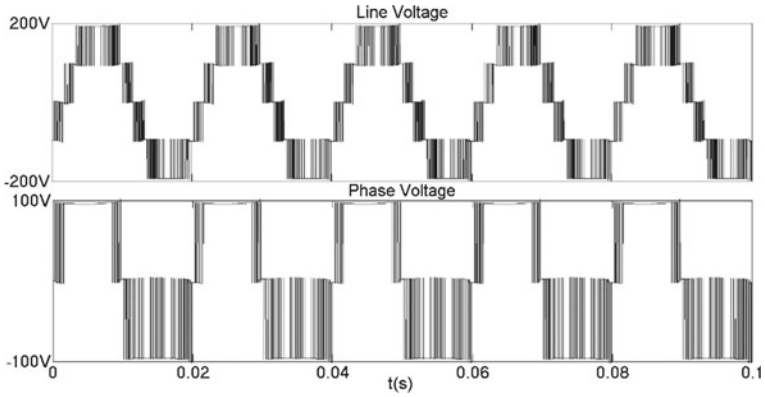
In 9-mode SVPWMs III and IV, three medium vectors and six small vectors are used, so the maximum amplitude of reference vector is $\frac{\sqrt{3}V_{dc}}{6}$. As a result, the maximum modulation index of 9-mode SVPWMs III and IV is

$$M = \frac{\pi V_{ref}}{2V_{dc}} = \frac{\pi \cdot \frac{\sqrt{3}}{6} V_{dc}}{2V_{dc}} = \frac{\sqrt{3}\pi}{12}, \quad \text{for 9-mode SVPWMs III and IV} \tag{7.54}$$

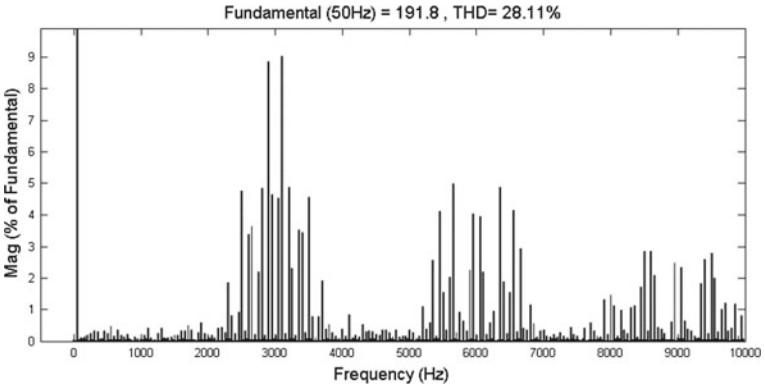
As six small vectors and six medium vectors are used in 12-mode SVPWM, the maximum modulation range is the regular hexagon surrounded by the medium vectors. Therefore, the maximum amplitude of reference vector is $\frac{V_{dc}}{2}$, and the maximum modulation index of 12-mode SVPWM is

$$M = \frac{\pi V_{ref}}{2V_{dc}} = \frac{\pi \cdot \frac{1}{2} V_{dc}}{2V_{dc}} = \frac{\pi}{4}, \quad \text{for 12-mode SVPWM} \tag{7.55}$$

The modulation range of 18-mode SVPWM is a regular hexagon formed by six large vectors, because six small vectors, six medium vectors, and six large vectors



(a) Line voltage and phase voltage.



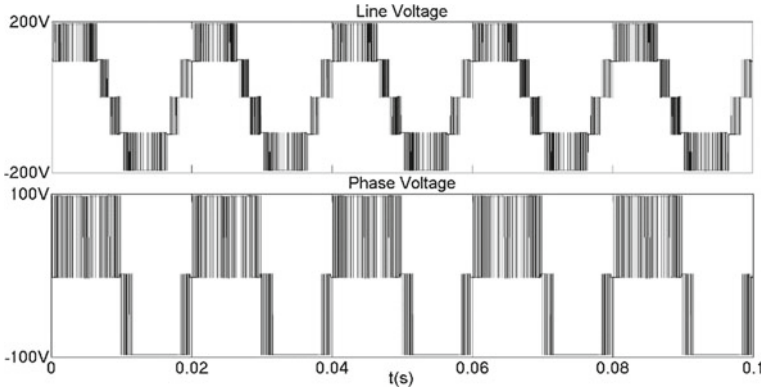
(b) FFT of line voltage.

Fig. 7.22 Simulation results of the diode-clamped three-level inverter with 18-mode SVPWM I

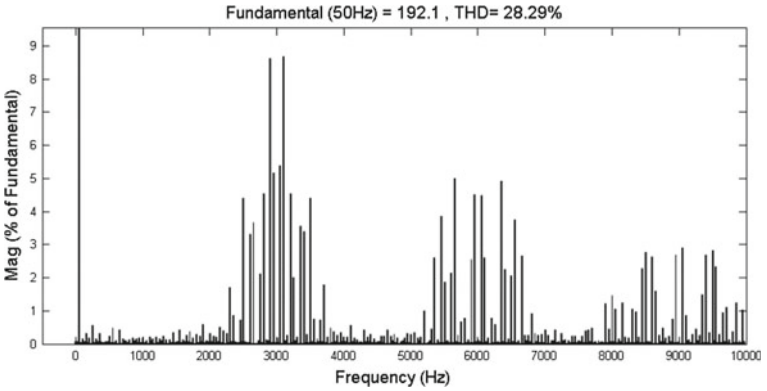
are adopted by 18-mode SVPWM. Therefore, the maximum amplitude of reference vector in 18-mode SVPWM is the same as that of conventional SVPWM, which is $\frac{\sqrt{3}}{3}V_{\mathrm{dc}}$ and the maximum index is

$$M = \frac{\pi V_{\mathrm{ref}}}{2V_{\mathrm{dc}}} = \frac{\pi \cdot \frac{\sqrt{3}}{3}V_{\mathrm{dc}}}{2V_{\mathrm{dc}}} = \frac{\sqrt{3}\pi}{6}, \quad \text{for 8-mode SVPWM} \tag{7.56}$$

The maximum modulation indexes of the diode-clamped three-level inverter with different SVPWM strategies are summarized in Table 7.9. It can be found that the DC voltage utilization of 18-mode SVPWM is the same as that of conventional SVPWM.



(a) Line voltage and phase voltage.

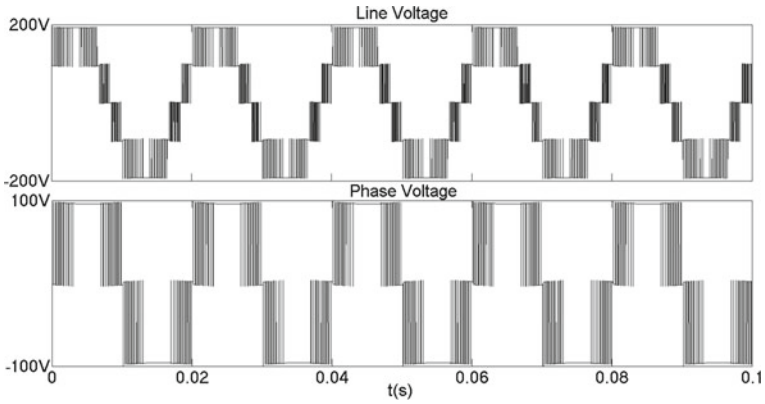


(b) FFT of line voltage.

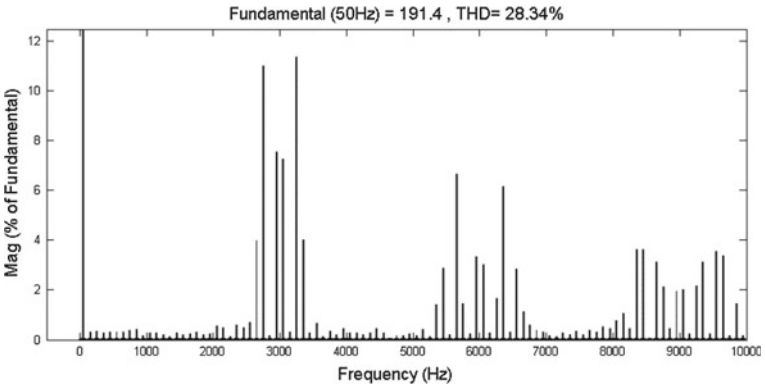
Fig. 7.23 Simulation results of the diode-clamped three-level inverter with 18-mode SVPWM II

Table 7.9 Comparison of maximum modulation index under different SVPWMs

Modulation strategy	Maximum modulation index
9-mode SVPWMs I and II	$\frac{\pi}{6}$
9-mode SVPWMs III and IV	$\frac{\sqrt{3}\pi}{12}$
12-mode SVPWM	$\frac{\pi}{4}$
18-mode SVPWM	$\frac{\sqrt{3}\pi}{6}$
Conventional SVPWM	$\frac{\sqrt{3}\pi}{6}$



(a) Line voltage and phase voltage.



(b) FFT of line voltage.

Fig. 7.24 Simulation results of the diode-clamped three-level inverter with 18-mode SVPWM III

7.4.2 Total Harmonic Distortion

When different SVPWM strategies are applied to the diode-clamped three-level inverter, the total harmonic content (THD) of the line voltage under different modulation indexes are listed in Table 7.10.

It can be seen from Table 7.10 that under the same modulation index, the 18-mode SVPWM has little difference from the conventional SVPWM in terms of total harmonic distortion of output line voltage. In addition, the 9-mode SVPWM is only available in low modulation indexes, and THDs of 9-mode SVPWM IIIs and IV are smaller than those of 9-mode SVPWMs I and II, because 9-mode SVPWMs III and IV use the medium vectors and small vectors to synthesize the required vector. When large modulation indexes are needed, only 12-mode SVPWM and 18-mode SVPWM can meet the requirements. However, THDs of 12-mode SVPWM is greater than

Table 7.10 Total harmonic distortion (%) of the output line voltage under different SVPWMs

Modulation strategy	$M =$ 0.9	$M =$ 0.8	$M =$ 0.7	$M =$ 0.6	$M =$ 0.5	$M =$ 0.4	$M =$ 0.3	$M =$ 0.2
9-mode SVPWM I	–	–	–	–	51.53	66.08	96.07	135.80
9-mode SVPWM II	–	–	–	–	51.56	66.08	96.07	135.80
9-mode SVPWM III	–	–	–	–	–	66.24	92.90	129.24
9-mode SVPWM IV	–	–	–	–	–	66.13	92.61	129.03
12-mode SVPWM	–	–	47.11	50.12	55.78	67.22	90.80	130.12
18-mode SVPWM I	26.98	33.86	38.56	41.93	45.61	65.69	94.95	134.08
18-mode SVPWM II	27.12	33.85	38.51	41.98	45.34	66.17	95.66	133.95
18-mode SVPWM III	27.34	33.78	38.60	41.91	44.79	63.78	90.77	130.02
Conventional SVPWM	26.94	33.72	38.60	41.98	46.30	68.36	94.67	130.14

those of 18-mode SVPWM, because large vectors are not used in 12-mode SVPWM to synthesize the required voltage vector.

7.4.3 Efficiency Analysis

The switching sequences and switching times of 18-mode SVPWM III and conventional SVPWM are listed in Table 7.11. It can be found that the 18-mode SVPWM does not use redundant small vectors, the operating modes involved are less than those of the conventional SVPWM, then the switching sequence is shorter and the number of switching times in the same small sector is reduced by 8 times from 12 times of the conventional SVPWM. Since the equivalent switching frequency can be reduced by using the 18-mode SVPWM, the efficiency of the inverter is improved correspondingly.

7.4.4 Experimental Verification

In order to verify the actual modulation effect of the 18-mode SVPWM III, the experimental parameters are given in Table 7.12. The phase and line voltages after filters are shown in Fig. 7.25. Although the phase voltage is a positive–negative

Table 7.11 Switching sequences and number of switching times under different SVPWMs (sector I)

Small sector	Conventional SVPWM	Num	Region	18-mode SVPWM III	Num
①	110-111-211-221-211-111-110	12	R_1	211-111-110-111-211	8
②	100-110-111-211-111-110-100	12	R_1	211-111-110-111-211	8
③	110-210-211-221-211-210-110	12	R_2	211-210-110-210-211	8
④	100-110-210-211-210-110-100	12	R_2	211-210-110-210-211	8
⑤	110-210-220-221-220-210-110	12	R_3	110-210-220-210-110	8
⑥	100-200-210-211-210-200-100	12	R_4	211-210-200-210-211	8
Total		72			48

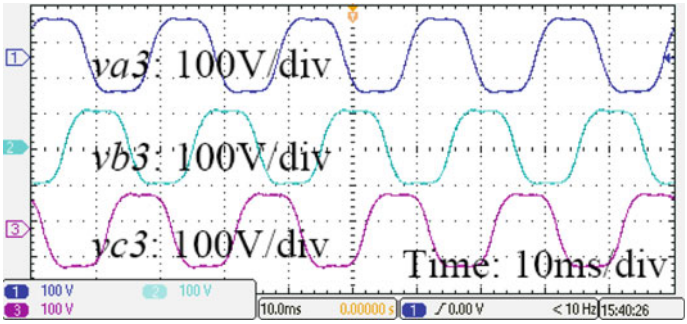
Table 7.12 Experimental parameters

Parameter	Value/part number
DC voltage	200 V
DC capacitance	1800 μF
Filter resistance	0.25 Ω
Filter inductance	2 mH
Filter capacitance	20 μF
Switching frequency	10 kHz
IGBT	BSM100GB60DLC
Clamped diode	MBR20200

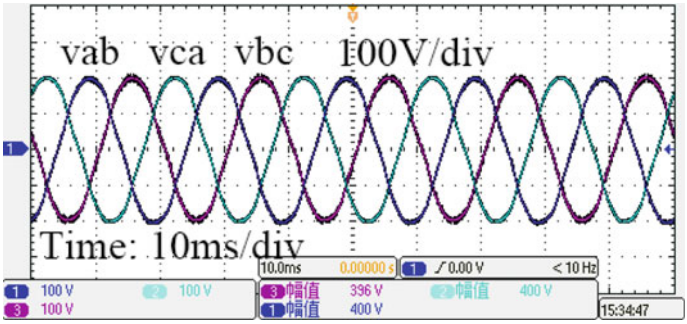
symmetrical flattop wave, the line voltage has a high sine degree, which verifies the feasibility of the proposed 18-mode SVPWM III.

The total harmonic distortion of the line voltage under different modulation indexes are listed in Table 7.13, it is found that THD of the 18-mode SVPWM III is similar to those of the conventional SVPWM. As shown in Fig. 7.26, under the maximum modulation index, the fundamental amplitude of the output voltage with 18-mode SVPWM is the same as that of the conventional SVPWM. The harmonic content of 18-mode SVPWM near the switching frequency is slightly higher than those of conventional SVPWM, but the harmonic contents at the high frequencies are smaller than those of the conventional SVPWM, which is important in reducing the EMI of the whole system.

When the three-phase diode-clamped three-level inverter feeds a three-phase four-wire resistive load, the output phase currents are proportional to the phase voltages.



(a) Phase voltage



(b) Line voltage

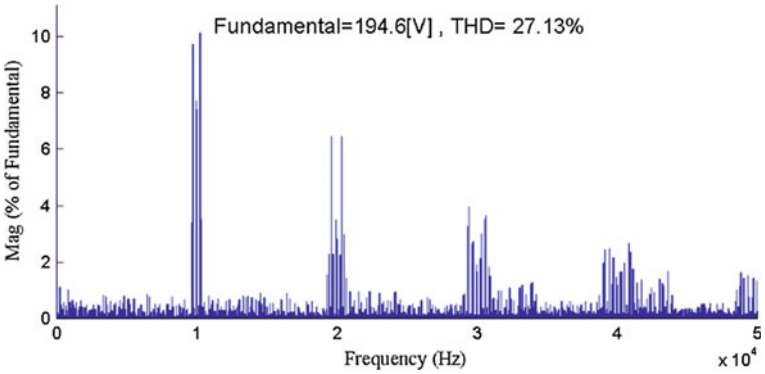
Fig. 7.25 Experimental waveforms of the diode-clamped three-level inverter with 18-mode SVPWM III (after filter)

Table 7.13 THD (%) of different modulation indexes

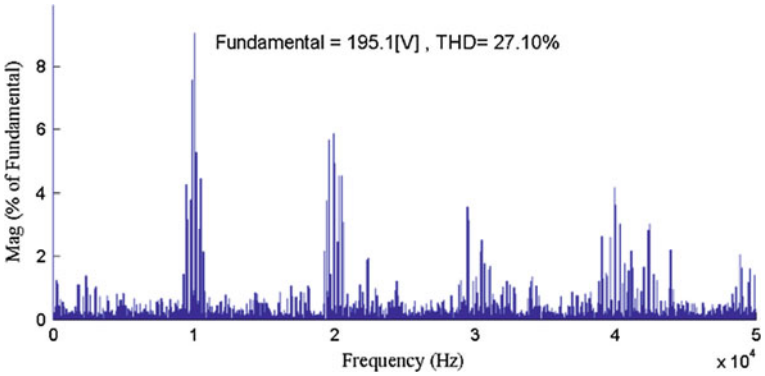
Modulation strategy	$M = 0.9$	$M = 0.8$	$M = 0.65$	$M = 0.5$	$M = 0.35$
18-mode SVPWM III	27.49	34.48	41.28	46.45	80.41
Conventional SVPWM	27.44	34.46	41.34	46.52	80.23

In order to avoid duplication of phase voltage and current waveforms, the output current waveform without filter and the DC current are depicted in Fig. 7.27.

Then, the efficiency of the three-phase diode-clamp three-level inverter can be calculated under different loads, which is shown in Fig. 7.28. Under the same load condition, since the switching frequency of the 18-mode SVPWM III is reduced by 1/3 compared with that of the conventional SVPWM, the switching loss of the switching device is reduced, and the overall efficiency is higher than that of the conventional SVPWM.



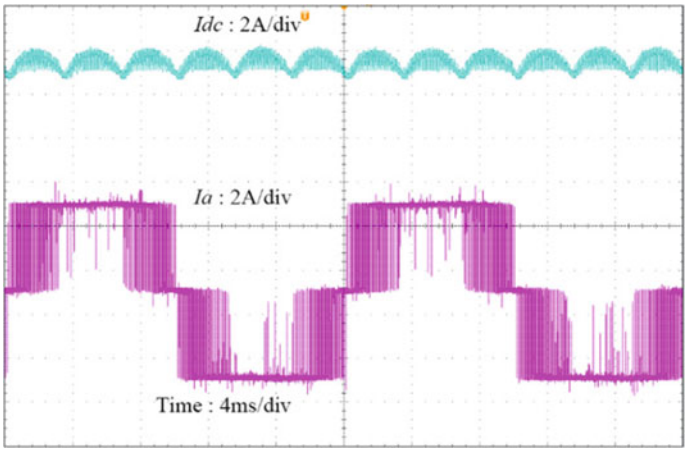
(a) *18*-mode SVPWM III.



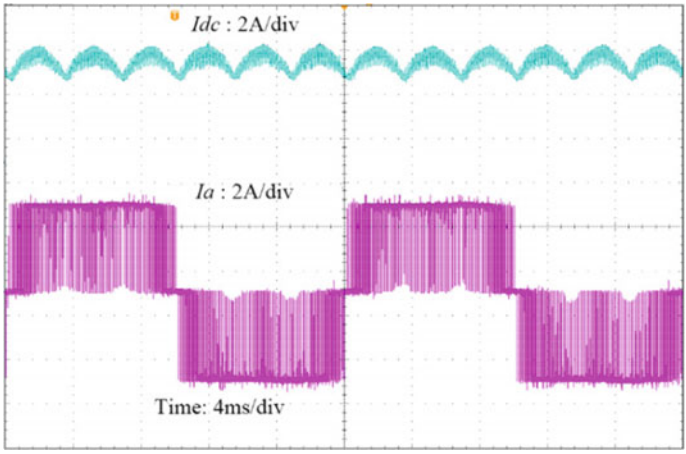
(b) Conventional SVPWM.

Fig. 7.26 FFT analysis of line voltage under different SVPWMs

It can be seen from the experimental results that the modulation range of the 18-mode SVPWM III is exactly the same as that of the conventional SVPWM; in terms of the total harmonic content of the output line voltage, both THDs are very close under different modulation indexes; in terms of inverter efficiency, due to the small number of operating modes used, the 18-mode SVPWM III under the same load condition has less switching times, lower loss, and higher efficiency; in terms of algorithm implementation, the 18-mode SVPWM III does not contain redundant operating mode, the algorithm is simple and the amount of calculation is reduced.



(a) *18*-mode SVPWM III.



(b) Conventional SVPWM.

Fig. 7.27 Experimental waveforms of dc current and output phase current under different SVPWMs

7.5 Summary

In this chapter, *m*-mode SVPWM method is first extended to the multilevel inverters. The three-phase diode-clamped three-level inverter is taken as an example to describe the controllability of *m*-mode SVPWM. Several typical *m*-mode SVPWM strategies are deduced in detail, including 3-mode SVPWMs, 6-mode SVPWMs, 9-mode SVPWMs, 12-mode SVPWMs, and 18-mode SVPWMs. The simulation and experimental results show that compared with the conventional SVPWM strategy,

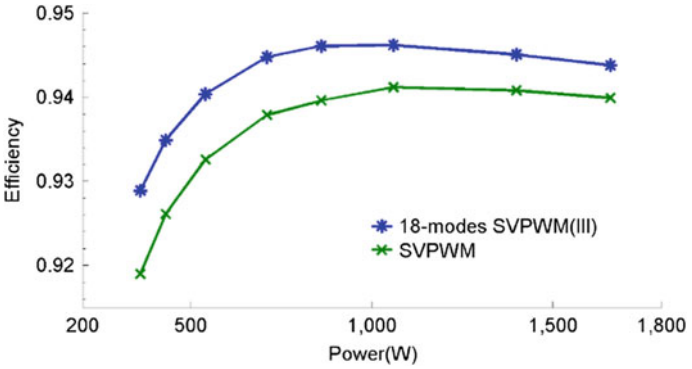


Fig. 7.28 Efficiency under different SVPWMs

the *m*-mode SVPWM strategy can effectively reduce the difficulty of the modulation strategy, simplify the switching sequence, and ultimately improve the efficiency of the inverter.

References

1. Nabae A, Takahashi I, Akagi H (1981) A new neutral-point-clamped PWM inverter. IEEE Trans Ind Appl IA-17(5):518–523
2. Meynard TA, Foch H (1992) Multi-level conversion: high voltage choppers and voltage-source inverters. In: 23rd Annual IEEE Power Electronics Specialists Conference
3. Corzine K, Familiant Y (2002) A new cascaded multilevel H-bridge drive. IEEE Trans Power Electron 17(1):125–131
4. Lai JS, Peng FZ (1996) Multilevel converters—a new breed of power converters. IEEE Trans Ind Appl 32(3):509–517
5. Seo JH, Choi CH, Hyun DS (2001) A new simplified space-vector PWM method for three-level inverters. IEEE Trans Power Electron 16(4):545–550
6. Jiang WD, Du SW, Chang LC et al (2010) Hybrid PWM strategy of SVPWM and VSVPWM for NPC three-level voltage-source inverter. IEEE Trans Power Electron 25(10):2607–2619
7. Kivanc OC, Ozturk SB (2017) Sector determination for SVPWM based four-switch three-phase VSI. Electron Lett 53(5):343–345
8. Ji Z, Wang L, Guo X (2008) On controllability of switched linear systems. IEEE Trans Autom Control 53(3):796–801
9. Wang W, Zhang B, Xie F (2018) A novel SVPWM for three-level NPC inverter based on m-Mode controllability. IEEE Trans Ind Electron 65(8):6055–6065

Chapter 8
m-Mode Controllability Applying to Modular Multilevel Converter

Modular multilevel converter (MMC) [1] is one kind of converters suitable for high voltage occasion. However, when the number of sub-modules increases as the voltage level increases, the SVPWM for MMC becomes very complex. Though using *m*-mode SVPWM can simplify the modulation strategy, a lot of calculation time is still needed in practice [2, 3]. Therefore, different from the previously proposed *m*-mode SVPWM strategies for inverters, this chapter first simplifies the topology of MMC sub-modules based on *m*-mode state controllability theory, thereby simplify the PWM strategy for MMC, which provides a new idea for the application of *m*-mode state controllability in the inverter.

8.1 *m*-Mode Controllability of Modular Multilevel Converter

A three-phase MMC inverter is shown in Fig. 8.1, in which several sub-modules are connected in series in each arm. There are mainly three types of sub-module: one is the full-bridge sub-module; the second is the half-bridge sub-module; the third is the clamped double-half-bridge sub-module. Among them, the most commonly used is the full-bridge sub-module.

When the full-bridge sub-module is used in MMC, the equivalent circuit of single-phase bridge arm is shown in Fig. 8.2. Since the full-bridge sub-module consists of four power switches, each of them include one IGBT and one antiparallel power diode, there are theoretically $2^4 = 16$ possible operating modes. Excluding the abnormal operating modes and the fault blocking operating modes, there are eight effective operating modes, which are listed in Table 8.1, and the corresponding equivalent circuits are shown in Fig. 8.3.

According to the aforementioned *m*-mode controllability theory of power converter, some operating modes of the converter can be selected to form a new switch-

B. Zhang and D. Qiu, *m-Mode SVPWM Technique for Power Converters*, CPSS Power Electronics Series, https://doi.org/10.1007/978-981-13-1382-0_8

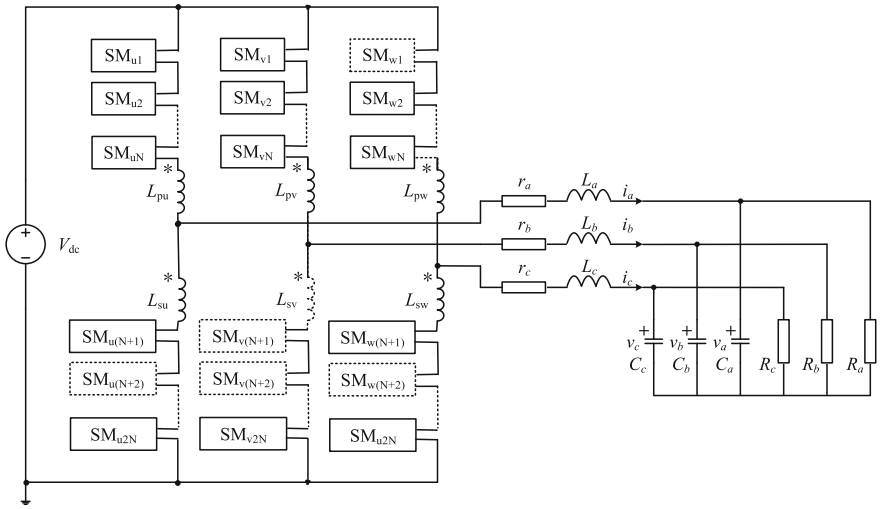


Fig. 8.1 Modular multilevel converter

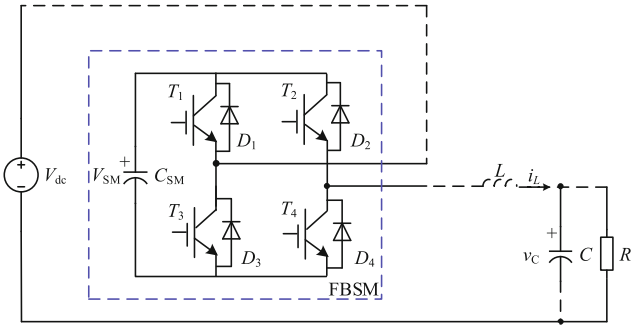
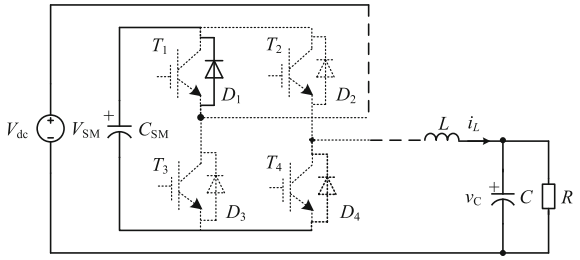


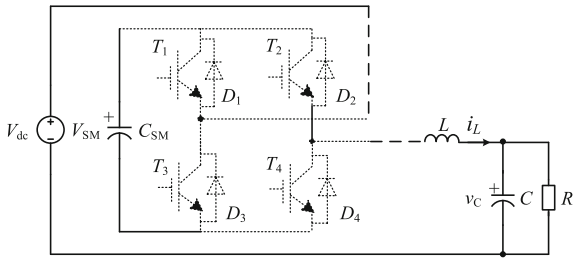
Fig. 8.2 Equivalent circuit of single-phase MMC bridge arm with full-bridge sub-module

Table 8.1 Operating modes and corresponding switching states of full-bridge sub-module

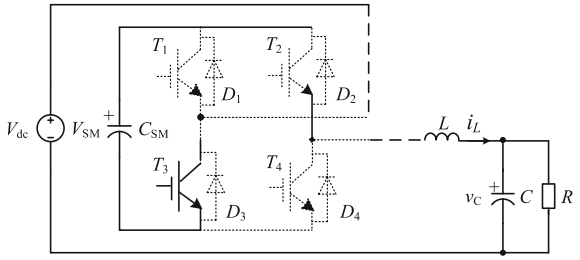
Mode	T_1	T_2	T_3	T_4	D_1	D_2	D_3	D_4	i_L	C_{SM}
1	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON	Positive	Charging
2	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	Negative	Charging
3	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	Positive	Discharging
4	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	Negative	Discharging
5	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	Positive	Bypass
6	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	Negative	Bypass
7	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	Positive	Bypass
8	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	Negative	Bypass



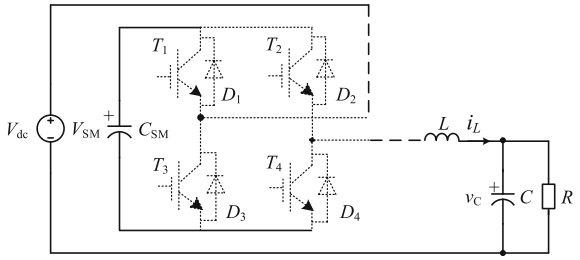
(a) Operating mode 1.



(b) Operating mode 2.



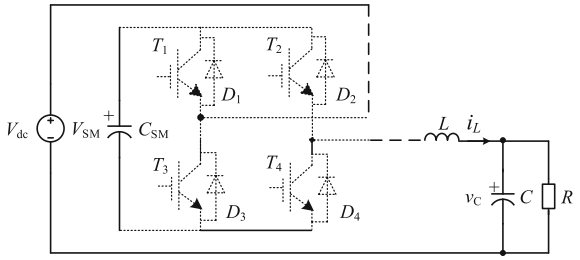
(c) Operating mode 3.



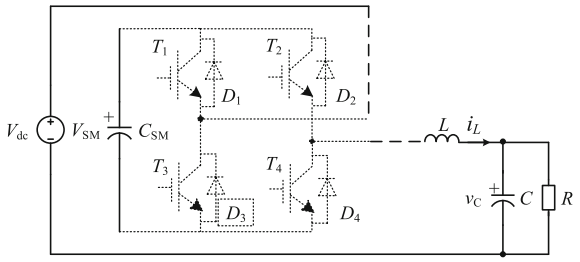
(d) Operating mode 4.

Fig. 8.3 Operating modes of single-phase MMC bridge arm with full-bridge sub-module

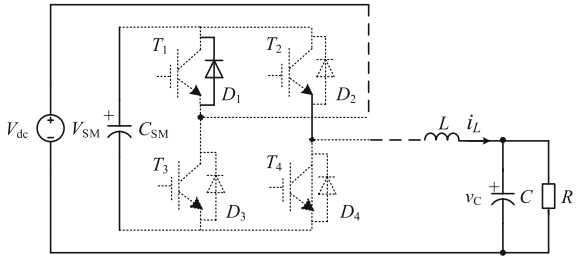
Fig. 8.3 (continued)



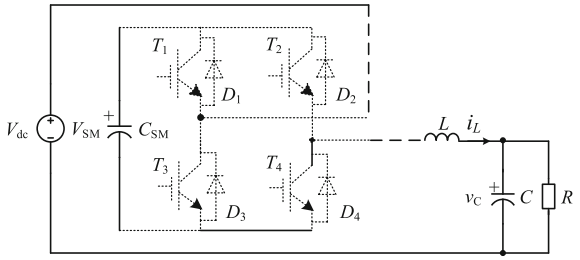
(e) Operating mode 5.



(f) Operating mode 6.



(g) Operating mode 7.



(h) Operating mode 8.

ing sequence, the converter is controllable if the rank of the corresponding switched linear model is equal to the number of state variables.

In order to analyze the controllability of MMC, the equivalent circuit of single-phase MMC bridge arm with full-bridge sub-module shown in Fig. 8.2 are taken as an example. The current i_L flowing through the filter inductor and the voltage v_c across the filter capacitor is selected as the state variables, which is $x = [i_L, v_c]^{\mathrm{T}}$. With respect to the operating principle of MMC and neglecting power feedback, four operating modes whose load current is positive are selected to form a new switching sequence with switching variable $\sigma \in (1, 3, 5, 7)$. The corresponding state equations are determined by

$$\begin{cases} V_{\mathrm{dc}} - V_{\mathrm{SM}} = L\frac{\mathrm{d}i_L}{\mathrm{d}t} + v_C \\ i_L = C\frac{\mathrm{d}v_C}{\mathrm{d}t} + \frac{v_C}{R} \end{cases}, \quad \text{for Mode 1} \tag{8.1}$$

$$\begin{cases} V_{\mathrm{dc}} + V_{\mathrm{SM}} = L\frac{\mathrm{d}i_L}{\mathrm{d}t} + v_C \\ i_L = C\frac{\mathrm{d}v_C}{\mathrm{d}t} + \frac{v_C}{R} \end{cases}, \quad \text{for Mode 3} \tag{8.2}$$

$$\begin{cases} V_{\mathrm{dc}} = L\frac{\mathrm{d}i_L}{\mathrm{d}t} + v_C \\ i_L = C\frac{\mathrm{d}v_C}{\mathrm{d}t} + \frac{v_C}{R} \end{cases}, \quad \text{for Modes 5 and 7} \tag{8.3}$$

Based on Eqs. (8.1)–(8.3), the state controllability matrix corresponding to Eq. (2.6) is constructed as below.

$$\begin{aligned} &[B_1, B_3, B_5, B_7, A_1B_1, \ldots, A_7B_1, \ldots, A_1B_7, \ldots, A_7B_7, \\ &A_1^2B_1, \ldots, A_1A_7B_1, \ldots, A_1^2B_7, \ldots, A_1A_7B_7, \ldots, \\ &A_1^3B_1, \ldots, A_1^2A_7B_1, \ldots, A_1^2A_7B_7, \ldots, A_7^3B_7] \end{aligned} \tag{8.4}$$

where

$$A_1 = A_3 = A_5 = A_7 = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \tag{8.5}$$

$$B_1 = \begin{bmatrix} \frac{V_{\mathrm{dc}} - V_{\mathrm{SM}}}{L} \\ 0 \end{bmatrix} \tag{8.6}$$

$$B_3 = \begin{bmatrix} \frac{V_{\mathrm{dc}} + V_{\mathrm{SM}}}{L} \\ 0 \end{bmatrix} \tag{8.7}$$

$$B_5 = B_7 = \begin{bmatrix} \frac{V_{\mathrm{dc}}}{L} \\ 0 \end{bmatrix} \tag{8.8}$$

Substituting Eqs. (8.5)–(8.8) into Eq. (8.4), it is obvious that $\widehat{B} = [B_1, B_3, B_5, B_7]$ is a matrix of non-full rank, $\widehat{A}_1 = \left[A_1\widehat{B}, A_3\widehat{B}, A_5\widehat{B}, A_7\widehat{B}\right]$ is of 2×4^2 dimensions,

and it is easy to calculate its rank is equal to the number of state variables of single-phase MMC bridge arm equivalent circuit, that is

$$\text{rank}\left[\widehat{A}_1\right] = p = 2 \tag{8.9}$$

Therefore, the single-phase MMC bridge arm equivalent circuit is state controllable, and it can be controlled only by operating modes 1, 3, 5, and 7.

8.2 Construction of Simplified MMC Sub-module Based on m-Mode Controllability

In the previous section, the m-mode controllability of MMC inverter has been proved and four operating modes (1, 3, 5, and 7) can achieve the control of system. Furthermore, it is found that not all switching devices are involved in the operating process, for example, switches T_1 and T_4 remain OFF, and diodes D_2 and D_3 remain OFF all the time. If some unused devices inside the full-bridge sub-module are removed, the MMC inverter is still controllable as long as the equivalent circuits or current paths corresponding to the operating modes 1, 3, 5, and 7 do not change. Therefore, the m-mode state controllability principle can be used to optimize the internal structure of the MMC sub-module, propose a new MMC sub-module structure to simplify the PWM strategy of the MMC inverter.

Based on the switching states corresponding to operating modes 1, 3, 5, and 7 listed in Table 8.1, the proposed simplified MMC sub-module is shown in Fig. 8.4 [4], which only has three power switches (or IGBTs) and one power diode. Compared with the full-bridge sub-module shown in Fig. 8.2, the original switch T_4, diodes D_2 and D_3 are removed, only the switches T_2, T_3, and diode D_3 is retained. As the states of diodes D_1 and D_4 are inconsistent in some operating modes, a fully controlled switch T_1 is used to replace diode D_1 and the connection direction of T_1 is opposite to that of the full-bridge sub-module.

Keeping the sub-module current i_{SM} be positive and considering the ON–OFF combination of switch devices, all operating modes of the simplified MMC sub-module can be obtained, the corresponding equivalent circuits are shown in Fig. 8.5 and the switching states are listed in Table 8.2.

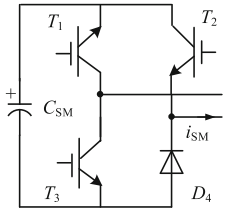
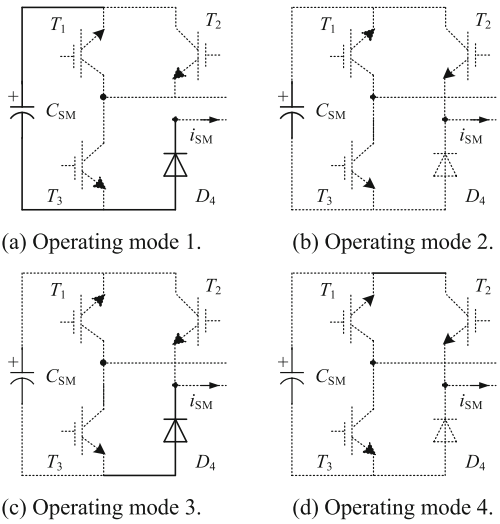


Fig. 8.4 Topology of the simplified MMC sub-module

Comparing Figs. 8.3 with 8.5, it can be found that in the operating mode shown in Fig. 8.5a, current i_{SM} flows through T_1 and D_1 and charges the module capacitor C_{SM}, corresponding to the operating mode 1 of full-bridge sub-module shown in Fig. 8.3a. In the operating mode shown in Fig. 8.5b, i_{SM} flows through T_3, T_2, and C_{SM} are discharged, corresponding to the operating mode 3 of full-bridge sub-module shown in Fig. 8.3c. In the operating mode shown in Fig. 8.5c, i_{SM} flows through T_3, D_1, and C_{SM} are bypassed, corresponding to mode 5 of full-bridge sub-module shown in Fig. 8.3e. In the operating mode shown in Fig. 8.5d, i_{SM} flows through T_1, T_2, and C_{SM} are bypassed too, corresponding to mode 7 of full-bridge sub-module shown in Fig. 8.3g. Consequently, the simplified MMC sub-module can achieve the function of full-bridge sub-module, and decrease the use of switching devices, which is beneficial to simplify the control of MMC.



(a) Operating mode 1. (b) Operating mode 2.

(c) Operating mode 3. (d) Operating mode 4.

Fig. 8.5 Equivalent circuits of the simplified MMC sub-module

Table 8.2 Operating modes and corresponding switching states of simplified MMC sub-module

Mode	T_1	T_2	T_3	D_4	i_{SM}	C_{SM}
1	ON	OFF	OFF	ON	Positive	Charging
2	OFF	ON	ON	OFF	Positive	Discharging
3	OFF	OFF	ON	ON	Positive	Bypass
4	ON	ON	OFF	OFF	Positive	Bypass

8.3 Topology and PWM Strategy of MMC with Simplified Sub-module

From the above analysis, the structure of the sub-module can be simplified based on the m-mode controllability of MMC inverter. By adopting the simplified MMC sub-module shown in Fig. 8.4, a new single-phase MMC inverter is shown in Fig. 8.6, in which the number of sub-modules in each arm is 2. Assuming that the rating voltage of sub-module capacitor C_{SM} is V_C, then the input voltage is $V_{\mathrm{dc}} = 2V_C$.

If the load is purely resistive, then the relationship among the load voltage v_{o}, input voltage V_{dc} and the output voltage of sub-module is expressed by

$$v_{\mathrm{o}} = V_{\mathrm{dc}} - (v_{\mathrm{SM1}} + v_{\mathrm{SM2}} + v_{\mathrm{SM7}} + v_{\mathrm{SM8}}) \tag{8.10}$$

or

$$v_{\mathrm{o}} = (v_{\mathrm{SM3}} + v_{\mathrm{SM4}} + v_{\mathrm{SM5}} + v_{\mathrm{SM6}}) - V_{\mathrm{dc}} \tag{8.11}$$

According to Eqs. (8.10) and (8.11), the load voltage is determined by the output voltages of the four sub-modules involved in the operation. Assuming that all sub-modules in operation only work in charging (discharging) or bypass state, which means that the sub-module output voltages are 0 and V_C, or 0 and $-V_C$. The rela-

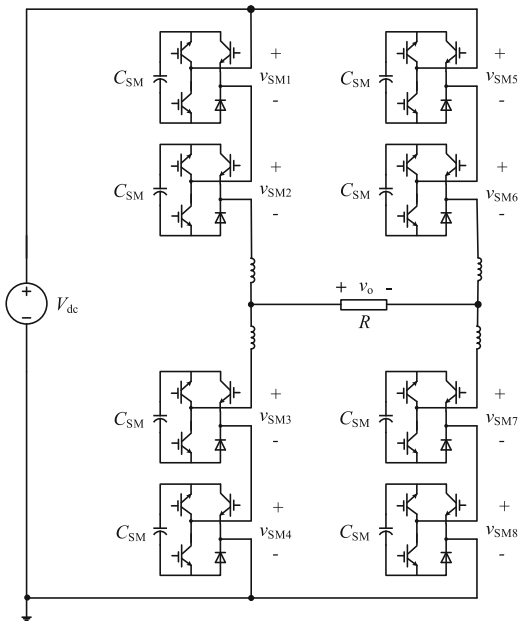


Fig. 8.6 Single-phase MMC with simplified sub-module

tionship between the load voltage and sub-module output voltages is summarized in Table 8.3.

Table 8.3 Output voltage of single-phase MMC inverter with simplified sub-module

v_{SM1}	v_{SM2}	v_{SM3}	v_{SM4}	v_{SM5}	v_{SM6}	v_{SM7}	v_{SM8}	v_o
$-V_C$	$-V_C$	–	–	–	–	$-V_C$	$-V_C$	$6V_C$
$-V_C$	$-V_C$	–	–	–	–	$-V_C$	0	$5V_C$
$-V_C$	$-V_C$	–	–	–	–	0	$-V_C$	$5V_C$
$-V_C$	0	–	–	–	–	$-V_C$	$-V_C$	$5V_C$
0	$-V_C$	–	–	–	–	$-V_C$	$-V_C$	$5V_C$
$-V_C$	$-V_C$	–	–	–	–	0	0	$4V_C$
$-V_C$	0	–	–	–	–	$-V_C$	0	$4V_C$
$-V_C$	0	–	–	–	–	0	$-V_C$	$4V_C$
0	$-V_C$	–	–	–	–	$-V_C$	0	$4V_C$
0	$-V_C$	–	–	–	–	0	$-V_C$	$4V_C$
0	0	–	–	–	–	$-V_C$	$-V_C$	$4V_C$
$-V_C$	0	–	–	–	–	0	0	$3V_C$
0	$-V_C$	–	–	–	–	0	0	$3V_C$
0	0	–	–	–	–	$-V_C$	0	$3V_C$
0	0	–	–	–	–	0	$-V_C$	$3V_C$
0	0	–	–	–	–	0	0	$2V_C$
V_C	V_C	–	–	–	–	0	0	0
V_C	0	–	–	–	–	V_C	0	0
V_C	0	–	–	–	–	0	V_C	0
0	V_C	–	–	–	–	V_C	0	0
0	V_C	–	–	–	–	0	V_C	0
0	0	–	–	–	–	V_C	V_C	0
–	–	V_C	V_C	0	0	–	–	0
–	–	V_C	0	V_C	0	–	–	0
–	–	V_C	0	0	V_C	–	–	0
–	–	0	V_C	V_C	0	–	–	0
–	–	0	V_C	0	V_C	–	–	0
–	–	0	0	V_C	V_C	–	–	0
–	–	V_C	0	0	0	–	–	$-V_C$
–	–	0	V_C	0	0	–	–	$-V_C$
–	–	0	0	V_C	0	–	–	$-V_C$
–	–	0	0	0	V_C	–	–	$-V_C$
–	–	0	0	0	0	–	–	$-2V_C$

(continued)

Table 8.3 (continued)

v_{SM1}	v_{SM2}	v_{SM3}	v_{SM4}	v_{SM5}	v_{SM6}	v_{SM7}	v_{SM8}	v_o
–	–	$-V_C$	0	0	0	–	–	$-3V_C$
–	–	0	$-V_C$	0	0	–	–	$-3V_C$
–	–	0	0	$-V_C$	0	–	–	$-3V_C$
–	–	0	0	0	$-V_C$	–	–	$-3V_C$
–	–	$-V_C$	$-V_C$	0	0	–	–	$-4V_C$
–	–	$-V_C$	0	$-V_C$	0	–	–	$-4V_C$
–	–	$-V_C$	0	0	$-V_C$	–	–	$-4V_C$
–	–	0	$-V_C$	$-V_C$	0	–	–	$-4V_C$
–	–	0	$-V_C$	0	$-V_C$	–	–	$-4V_C$
–	–	0	0	$-V_C$	$-V_C$	–	–	$-4V_C$
–	–	$-V_C$	$-V_C$	$-V_C$	0	–	–	$-5V_C$
–	–	$-V_C$	$-V_C$	0	$-V_C$	–	–	$-5V_C$
–	–	$-V_C$	0	$-V_C$	$-V_C$	–	–	$-5V_C$
–	–	0	$-V_C$	$-V_C$	$-V_C$	–	–	$-5V_C$
–	–	$-V_C$	$-V_C$	$-V_C$	$-V_C$	–	–	$-6V_C$

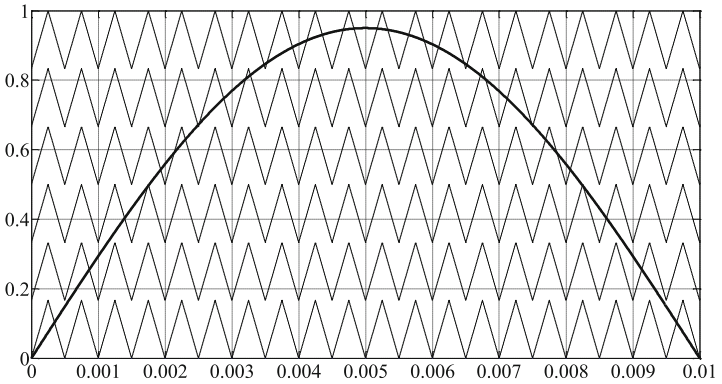


Fig. 8.7 PWM strategy for the proposed MMC

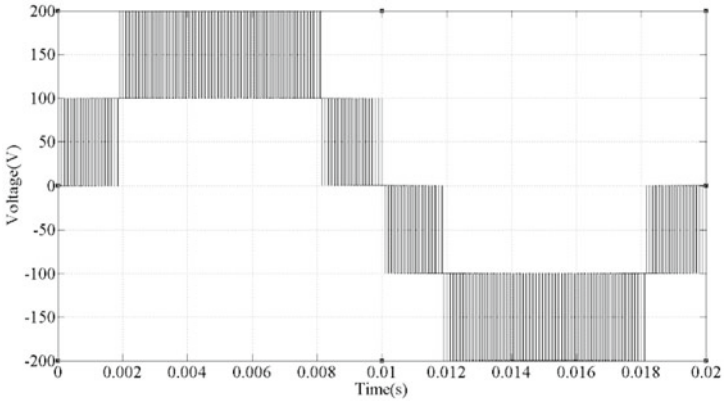
From Table 8.3, there are six positive and negative levels of the output voltage for single-phase MMC shown in Fig. 8.6. By considering the zero voltage level, there are 13 levels in total, that is, the single-phase MMC with simplified sub-module can output 13 levels.

If the carrier disposition PWM is used, the positive half cycle of the sinusoidal reference and the triangular carrier waveforms are shown in Fig. 8.7, where the amplitude of the sinusoidal reference ranges from −1 to +1. Since there are six voltage intervals of the output voltage in the positive half cycle, which are 0–V_C, V_C–$2V_C$, …, and $5V_C$–$6V_C$, six triangular carrier signals are needed. The relevant switches in the

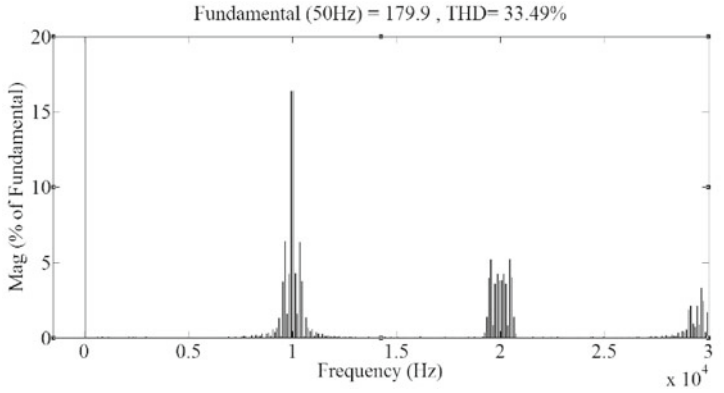
sub-module are driven according to the comparison results of the sinusoidal reference and the carrier signals. For the negative half cycle of the sinusoidal reference, the triangular carriers should be reversed.

8.4 Simulation Results

In order to verify the correctness of the above theoretical analysis, a simulation model of single-phase MMC inverter based on Fig. 8.6 are constructed in MATLAB/Simulink. The simulation parameters are set as follows: DC input voltage $V_{dc} = 2V_C = 200$ V, load resistance $R = 200\ \Omega$, output fundamental frequency $f = 50$ Hz, and carrier frequency $f_c = 10$ kHz.

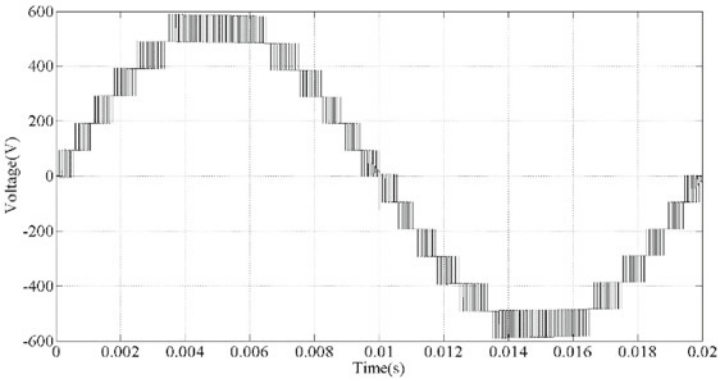


(a) Output voltage waveform.

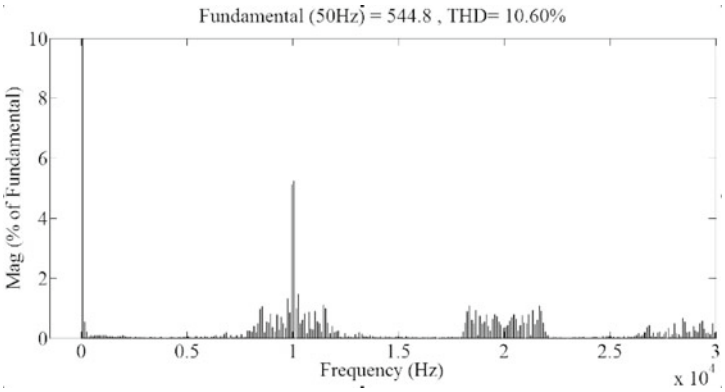


(b) FFT analysis of the output voltage.

Fig. 8.8 Five-level output voltage of single-phase MMC with simplified sub-module



(a) Output voltage waveform.



(b) FFT analysis of the output voltage.

Fig. 8.9 Thirteen-level output voltage of single-phase MMC with simplified sub-module

When modulating the single-phase MMC inverter to output only five levels, the simulation waveforms are shown in Fig. 8.8. The maximum output voltage is equal to the DC input voltage (200 V), and the total harmonic distortion of the output voltage is as high as 33.49%.

When modulating single-phase MMC inverter to output 13 levels, the output voltage waveform in Fig. 8.9a has the maximum amplitude which reaches three times of the DC input voltage (600 V). The spectrum analysis of the output voltage results in the total harmonic distortion rate of only 10.60% as shown in Fig. 8.9b, which is much lower than that of the five-level output.

8.5 Summary

Based on the *m*-mode controllability theory, this chapter discusses the topology optimization method of power electronic converters. Taking the MMC converter as an example, the *m*-mode controllability of the full-bridge sub-module is carried out, which proves that the full-bridge sub-module is 4-mode controllable. According to the controllability result of the full-bridge sub-module, together with the selected operating modes of the full-bridge sub-module, a new MMC simplified sub-module is put forward. Compared with the conventional MMC full-bridge sub-module, the designed MMC simplified sub-module reduces the use of one power switch, thus simplifies the modulation strategy, reduces the amount of calculation and shortens the calculation time, which provides a new idea in applying *m*-mode controllability to multilevel inverters.

References

1. Lesnicar A, Marquardt R (2003) An innovative modular multilevel converter topology suitable for a wide power range. IEEE Bologna Power Tech Conf Proc 3:3–6
2. Tang G, Xu Z, Zhou Y (2014) Impacts of three MMC-HVDC configurations on AC system stability under DC line faults. IEEE Trans Power Systems 29(6):3030–3040
3. Ou K, Rao H, Cai Z (2014) MMC-HVDC simulation and testing based on real-time digital simulator and physical control system. IEEE J Emerg Sel Top Power Electron 2(4):1109–1116
4. Li X, Zhang B, Zhang Z et al (2017) A novel MMC sub-module based on controllability theory. In: 43rd annual conference of the IEEE industrial electronics society, pp 4829–4833

Chapter 9
m-Mode SVPWM for PWM Rectifier

The previous chapters have discussed the application of *m*-mode SVPWM in different types of inverters. In fact, *m*-mode SVPWM is also applicable to other converters that adopt PWM strategy. In this chapter, *m*-mode SVPWM is extended to voltage-source PWM rectifier. According to the operating principle of PWM rectifier, the switched linear system model of PWM rectifier is established, and the condition of *m*-mode controllability is obtained based on the state controllability criterion of power converter. Then, *m*-mode SVPWMs suitable for PWM rectifier is put forward and verified by simulation results.

9.1 Overview of PWM Rectifier

9.1.1 Topology of PWM Rectifier

In 1979, the PWM concept of AC/DC converters was first proposed [1]. Subsequently, a three-phase full-bridge AC/DC converter using fully controlled switching devices was proposed to achieve the unity power factor operation and AC sinusoidal input current by PWM [2].

The common topologies of voltage-source PWM rectifier are shown in Figs. 9.1, 9.2, and 9.3, including single-phase rectifier in Fig. 9.1, three-phase rectifier in Fig. 9.2, and three-phase three-level rectifier in Fig. 9.3. Although the three-phase three-level rectifier is suitable for high voltage applications, the number of required power switches is increased and the control is relatively complicated. Therefore, this chapter will take the three-phase voltage-source PWM rectifier shown in Fig. 9.2 as the example, to explore the application of *m*-mode SVPWM in PWM rectifiers.

B. Zhang and D. Qiu, *m-Mode SVPWM Technique for Power Converters*, CPSS Power Electronics Series, https://doi.org/10.1007/978-981-13-1382-0_9

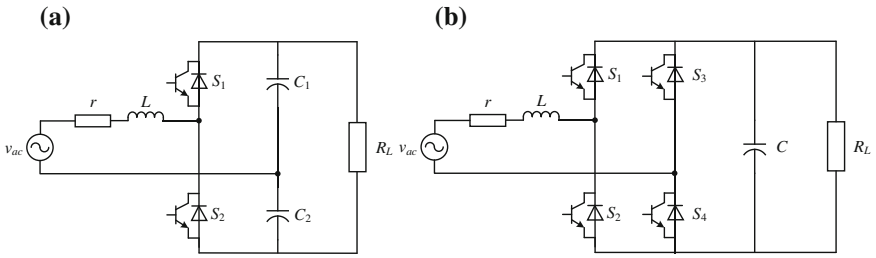


Fig. 9.1 Single-phase voltage-source rectifier **a** half-bridge, **b** full-bridge

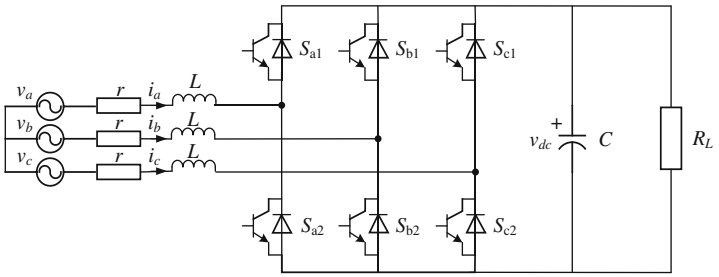


Fig. 9.2 Three-phase voltage-source rectifier

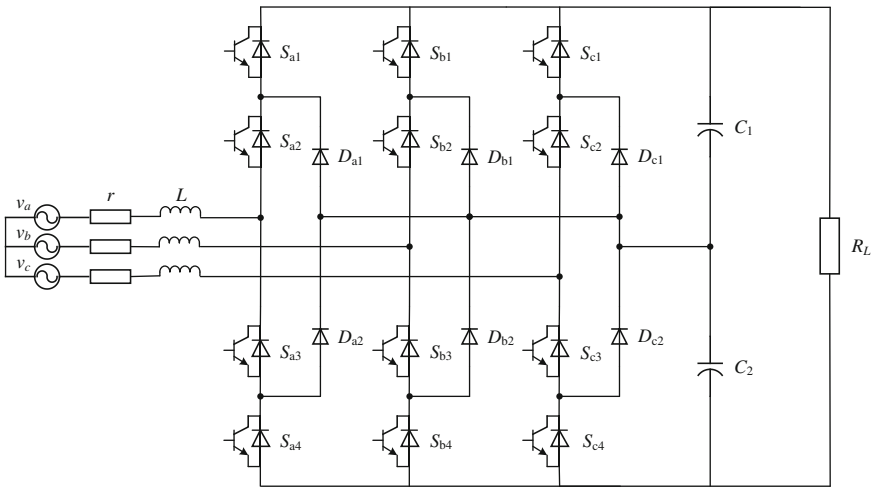


Fig. 9.3 Three-phase three-level voltage-source rectifier

9.1.2 Operating Principle of PWM Rectifier

By applying PWM to control the fully controlled switching devices of the voltage-source rectifier, not only the desired magnitude of the rectified voltage can be obtained, but also the input current can be changed in a sinusoidal manner approximately. If the input inductance L is large enough, for the convenience of analysis, only the fundamental component of the AC side voltage of the PWM rectifier is considered, and the AC side resistance is ignored, then the equivalent circuit of the voltage-source PWM rectifier is shown in Fig. 9.4. Since $v_{ac} = v_L + v_{in}$, if the AC power supply voltage at the grid side v_{ac} does not change, then the amplitude and phase of the input inductor current (or input current) i_L are determined by the fundamental component v_{in1} of the AC side voltage v_{in} of the rectifier and the AC power supply voltage v_{ac}. Therefore, by controlling the turn-on and turn-off of the power switcher, and thus controlling the amplitude and phase of the voltage fundamental component of the rectifier AC side, the output voltage and power factor of the rectifier can be controlled.

Under the steady-state conditions, the vector relationship between the voltage and current of the rectifier AC side is shown in Fig. 9.5, where the AC power supply voltage vector $\vec{V}_{ac}$ is the reference vector (line segment $O'O$). By controlling the voltage vector of the rectifier AC side $\vec{V}_{in}$ (line segment $O'X$, $X = A, B, C, D$), the amplitude of the input current $\left|\vec{I}_L\right|$ or inductor voltage $\left|\vec{V}_L\right| = \omega L\left|\vec{I}_L\right|$) can keep constant. At this time, the trajectory of the end point X of fundamental voltage vector $\vec{V}_{in1}$ forms a circle with radius $\left|\vec{V}_L\right|$, which means that the rectifier can operate in four quadrants. Figure 9.5a–d represent four different operating modes, namely positive resistor, negative resistor, pure inductor, and pure capacitor, respectively.

As shown in Fig. 9.5a, the end point of $\vec{V}_{in1}$ locates at point A, that is, v_{in1} lags v_{ac} by a certain angle, to make v_L lead v_{ac} by 90°. Since the inductor current lags the inductor voltage by 90°, the inductor current (or input current) i_L is in phase with v_{ac}, and the rectifier exhibits positive resistor operating characteristic as a whole.

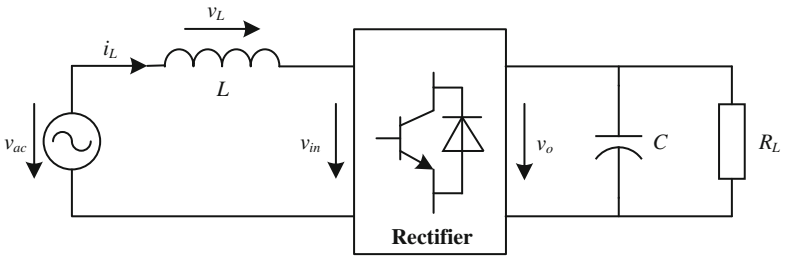


Fig. 9.4 Equivalent circuit of a PWM rectifier

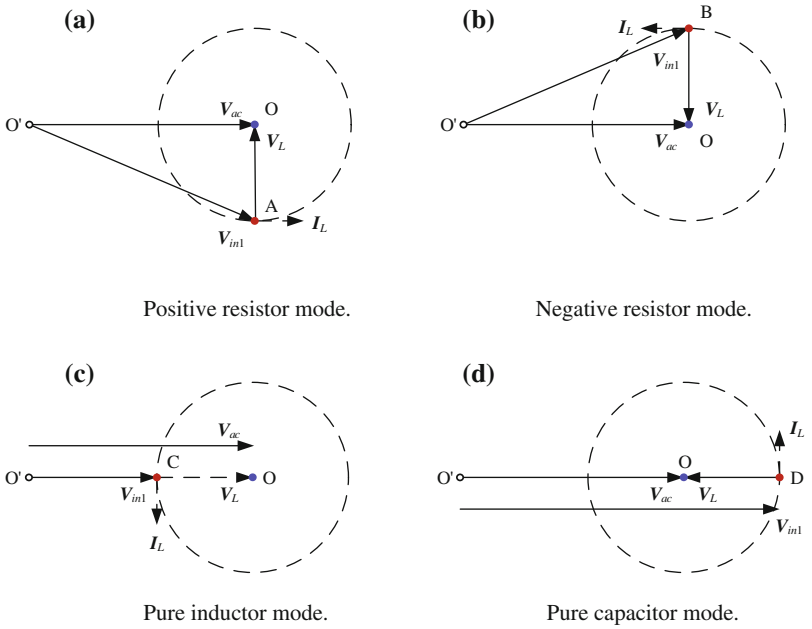


Fig. 9.5 Phasor diagram of PWM rectifier under different operating modes

As shown in Fig. 9.5b, the end point of $\vec{V}_{\text{in1}}$ locates at point B, that is, v_{in1} leads v_{ac} by a certain angle, so that v_L lags v_{ac} by 90°, and the input current i_L is opposite to the AC power supply voltage v_{ac}. Consequently, the rectifier exhibits negative resistor operating characteristic.

As shown in Fig. 9.5c, the end point of $\vec{V}_{\text{in1}}$ locates at point C, that is, v_{in1} is in phase with v_{ac} but its amplitude is less than that of v_{ac}. At this time, v_L is in phase with v_{ac} as well, and the input current i_L lags the AC power supply voltage v_{ac} by 90°. Therefore, the rectifier exhibits pure inductor operation characteristics.

As shown in Fig. 9.5d, the end point of $\vec{V}_{\text{in1}}$ locates at point D, that is, v_{in1} is in phase with the grid voltage v_{ac} but its amplitude is greater than that of v_{ac}. At this time, v_L is opposite to v_{ac}, and the input current i_L leads the AC power supply voltage v_{ac} by 90°. Thus, the rectifier exhibits pure capacitor operating characteristics.

The above four operating modes are special cases of PWM rectifier. In most cases, the input current vector of the rectifier can be placed in any quadrant to achieve four-quadrant operation of the rectifier by adjusting the amplitude and phase of the AC side voltage of the rectifier. As shown in Fig. 9.5, the control of the rectifier input current can be achieved by controlling the voltage of the rectifier. Currently, the main modulation methods of the PWM rectifier include carrier PWM technology and SVPWM technology. The *m*-mode SVPWM for PWM rectifier will be discussed in next section.

9.2 *m*-Mode SVPWM Strategy

9.2.1 Switched Linear System Model

As shown in Fig. 9.2, the three-phase voltage-source PWM rectifier consists of three-phase bridge arms. Each phase bridge arm has two switching states, so there are eight combinations of switching states. Each switching state combination corresponds to one operating mode or voltage vector. Similar to the three-phase four-wire inverter, all the switching states and operating modes of the three-phase voltage-source PWM rectifier are listed in Table 9.1.

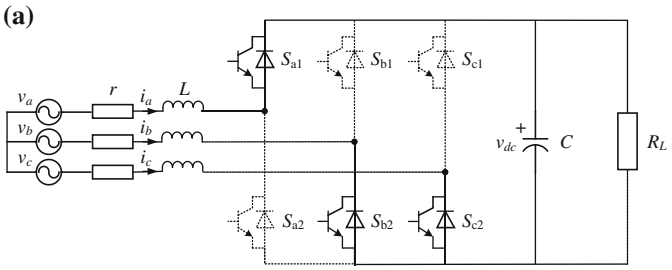
According to the switching states in Table 9.1, the equivalent circuits corresponding to the eight operating modes of the three-phase voltage-source PWM rectifier can be obtained in Fig. 9.6.

The three-phase input currents (or inductor currents) i_a, i_b, i_c and the DC side capacitor voltage v_{dc} are selected as the state variables, that is, $x = [i_a, i_b, i_c, v_{\mathrm{dc}}]^{\mathrm{T}}$. According to Fig. 9.6, the switched linear system model similar to Eq. (2.1) with switching variable $\sigma \in (1, 2, \cdots, 8)$ can be obtained, where

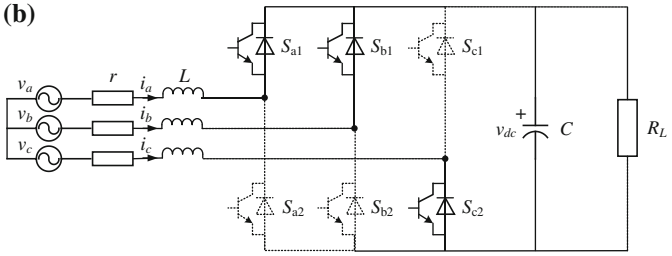
$$A_1 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{2}{3L} \\ 0 & -\frac{r}{L} & 0 & \frac{1}{3L} \\ 0 & 0 & -\frac{r}{L} & \frac{1}{3L} \\ \frac{1}{C} & 0 & 0 & -\frac{1}{R_L C} \end{bmatrix} \tag{9.1}$$

Table 9.1 Operating modes of the three-phase voltage-source PWM rectifier

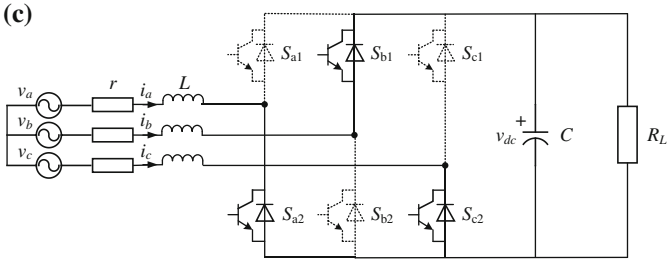
Mode	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	Vector	Binary representation
1	ON	OFF	OFF	OFF	ON	ON	$\vec{V}_{s1}$	100
2	ON	ON	OFF	OFF	OFF	ON	$\vec{V}_{s2}$	110
3	OFF	ON	OFF	ON	OFF	ON	$\vec{V}_{s3}$	010
4	OFF	ON	ON	ON	OFF	OFF	$\vec{V}_{s4}$	011
5	OFF	OFF	ON	ON	ON	OFF	$\vec{V}_{s5}$	001
6	ON	OFF	ON	OFF	ON	OFF	$\vec{V}_{s6}$	101
7	OFF	OFF	OFF	ON	ON	ON	$\vec{V}_{s7}$	000
8	ON	ON	ON	OFF	OFF	OFF	$\vec{V}_{s8}$	111



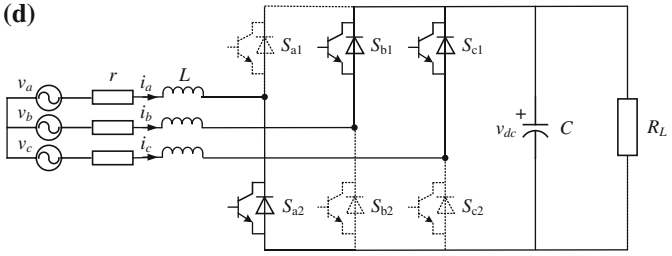
Operating mode 1 (100).



Operating mode 2 (110).



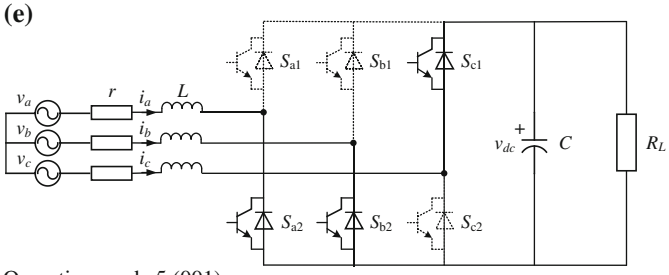
Operating mode 3 (010).



Operating mode 4 (011).

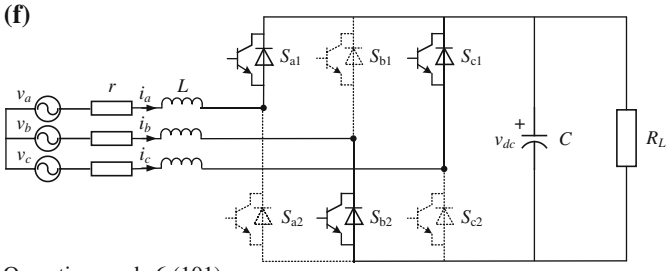
Fig. 9.6 Equivalent circuits of three-phase voltage-source PWM rectifier

(e)



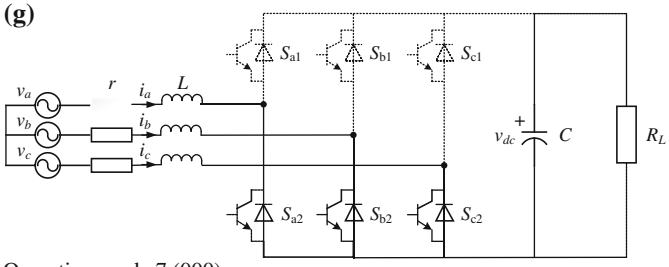
Operating mode 5 (001).

(f)



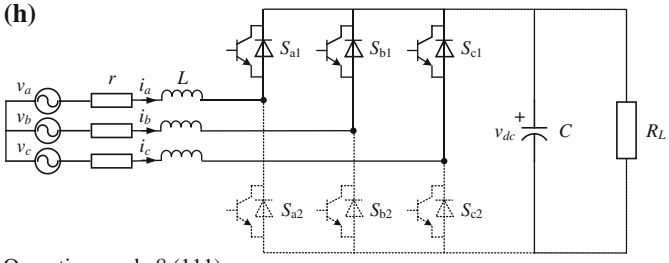
Operating mode 6 (101).

(g)



Operating mode 7 (000).

(h)



Operating mode 8 (111).

Fig. 9.6 (continued)

$$A_2 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{1}{3L} \\ 0 & -\frac{r}{L} & 0 & -\frac{1}{3L} \\ 0 & 0 & -\frac{r}{L} & \frac{2}{3L} \\ \frac{1}{C} & \frac{1}{C} & 0 & -\frac{1}{R_L C} \end{bmatrix} \tag{9.2}$$

$$A_3 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{1}{3L} \\ 0 & -\frac{r}{L} & 0 & -\frac{1}{3L} \\ 0 & 0 & -\frac{r}{L} & \frac{1}{3L} \\ 0 & \frac{1}{C} & 0 & -\frac{1}{R_L C} \end{bmatrix} \tag{9.3}$$

$$A_4 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & \frac{2}{3L} \\ 0 & -\frac{r}{L} & 0 & -\frac{1}{3L} \\ 0 & 0 & -\frac{r}{L} & -\frac{1}{3L} \\ 0 & \frac{1}{C} & \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix} \tag{9.4}$$

$$A_5 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & \frac{1}{3L} \\ 0 & -\frac{r}{L} & 0 & \frac{1}{3L} \\ 0 & 0 & -\frac{r}{L} & -\frac{2}{3L} \\ 0 & 0 & \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix} \tag{9.5}$$

$$A_6 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & -\frac{1}{3L} \\ 0 & -\frac{r}{L} & 0 & \frac{2}{3L} \\ 0 & 0 & -\frac{r}{L} & -\frac{1}{3L} \\ \frac{1}{C} & 0 & \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix} \tag{9.6}$$

$$A_7 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & 0 \\ 0 & -\frac{r}{L} & 0 & 0 \\ 0 & 0 & -\frac{r}{L} & 0 \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & -\frac{1}{R_L C} \end{bmatrix} \tag{9.7}$$

$$A_8 = \begin{bmatrix} -\frac{r}{L} & 0 & 0 & 0 \\ 0 & -\frac{r}{L} & 0 & 0 \\ 0 & 0 & -\frac{r}{L} & 0 \\ 0 & 0 & 0 & -\frac{1}{R_L C} \end{bmatrix} \tag{9.8}$$

$$B_1 = \cdots = B_8 = \begin{bmatrix} \frac{1}{L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L} \\ 0 & 0 & 0 \end{bmatrix} \tag{9.9}$$

9.2.2 m-*Mode Controllability*

According to controllability criterion 2.1 for power converter, the controllability analysis of the three-phase voltage-source PWM rectifier is carried out in this section. Since the operating modes 7 and 8 represent for the zero voltage vector, the number of effective operating modes is 6, and the matrix corresponding to Eq. (2.6) is constructed as below.

$$[B_1, \ldots, B_6, A_1B_1, \ldots, A_1B_6, \ldots, A_6B_1, \ldots, A_6B_6,$$
$$A_1^2B_1, \ldots, , A_1^2B_6, \ldots, A_1A_6B_1, \ldots A_1A_6B_6, \ldots,$$
$$A_1^5B_1, \ldots A_1^5B_6, \ldots, A_1A_6^4B_6, \ldots, A_6^5B_6] \tag{9.10}$$

Based on Eqs. (9.1)–(9.9), it is obvious that $\widehat{B} = [B_1, B_2, \ldots, B_6]$ is a non-full rank matrix, while $A_1\widehat{B} = [A_1B_1, \ldots, A_1B_6]$ is a matrix of 4×18 dimensions, and it is easy to calculate its rank equal to the number of state variables of the PWM rectifier, that is

$$\text{rank}\,[A_1\widehat{B}] = p = 4 \tag{9.11}$$

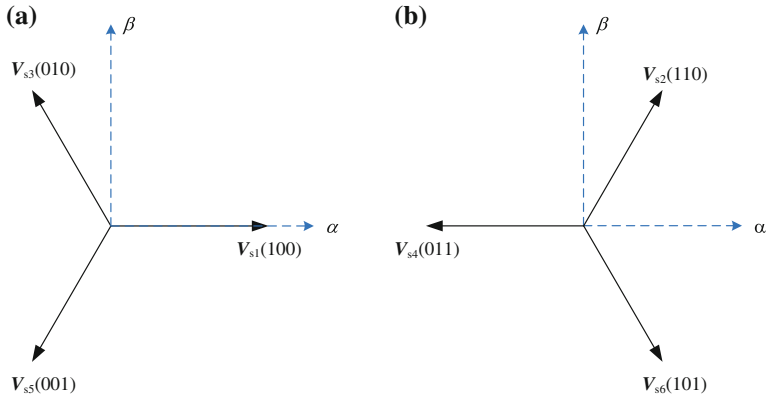
Therefore, Eq. (9.11) indicates that the three-phase PWM rectifier is state controllable.

9.2.3 m-*Mode SVPWM*

Referring to the 3-mode SVPWM for the three-phase four-wire inverter, if only the operating modes 1, 3, and 5 are selected to modulate the three-phase PWM rectifier, then the controllability criterion of PWM rectifier can be calculated as below.

$$\text{rank}\,[B_1, B_3, B_5, A_1B_1, A_3B_1, A_5B_1, \ldots, A_1B_5, A_3B_5, A_5B_5] = 4 \tag{9.12}$$

Equation (9.12) means the three-phase PWM rectifier is 3-mode controllable.



3-mode SVPWM I. *3*-mode SVPWM II.

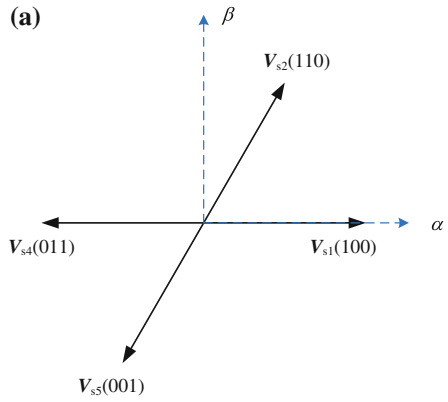
Fig. 9.7 Vector distribution of 3-mode SVPWM

Similarly, if only operating modes 2, 4, and 6 are selected to modulate the PWM rectifier, then we have

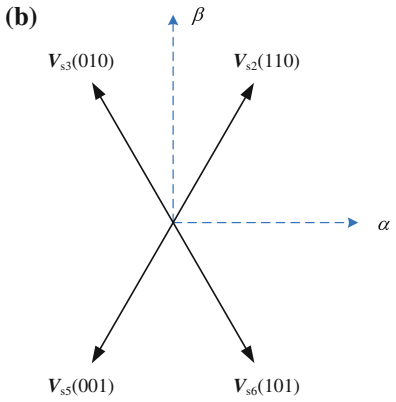
$$\text{rank}\,[B_2, B_4, B_6, A_2B_2, A_4B_2, A_6B_2, \ldots, A_2B_6, A_4B_6, A_6B_6] = 4 \tag{9.13}$$

The above equation also proves that the three-phase PWM rectifier is 3-mode controllable.

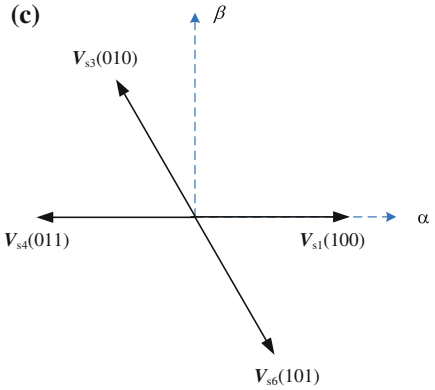
Therefore, the three-phase PWM rectifier can be controlled by the operating modes 1, 3, and 5, or 2, 4 and 6. The following switching strategy using operating modes 1, 3, and 5 is called 3-mode SVPWM I, while the one using modes 2, 4, and 6 are called 3-mode SVPWM II, and their corresponding space vectors are distributed as shown in Fig. 9.7.



4-mode SVPWM I.



4-mode SVPWM II.



4-mode SVPWM III.

Fig. 9.8 Vector distribution of 4-mode SVPWMs

According to the 4-mode controllability of the three-phase four-wire inverter, there are three types of 4-mode combinations for the three-phase PWM rectifier, including modes 1, 2, 4, and 5, modes 2, 3, 5,and 6, and modes 1, 3, 4, and 6. Then, the 4-mode controllability matrixes of the three-phase PWM rectifier are constructed respectively, and their ranks are calculated as below.

$$\text{rank}\,[B_1, B_2, B_4, B_5, A_1B_1, \ldots, A_5B_1, \ldots, A_1B_5, \ldots, A_5B_5] = 4 \tag{9.14}$$

$$\text{rank}\,[B_2, B_3, B_5, B_6, A_2B_2, \ldots, A_6B_2, \ldots, A_2B_6, \ldots, A_6B_6] = 4 \tag{9.15}$$

$$\text{rank}\,[B_1, B_3, B_4, B_6, A_1B_1, \ldots, A_6B_1, \ldots, A_1B_6, \ldots, A_6B_6] = 4 \tag{9.16}$$

Equations (9.14)–(9.16) indicate that the three-phase PWM rectifier is 4-mode controllable. The voltage space vector distribution of the above three 4-mode SVPWMs is shown in Fig. 9.8. The voltage space vector synthesis method corresponding to the operating modes 1, 2, 4, and 5 is called 4-mode SVPWM I; the synthesis method adopting modes 2, 3, 5, and 6 is called 4-mode SVPWM II; and the synthesis method using modes 1, 3, 4, and 6 is called 4-mode SVPWM III.

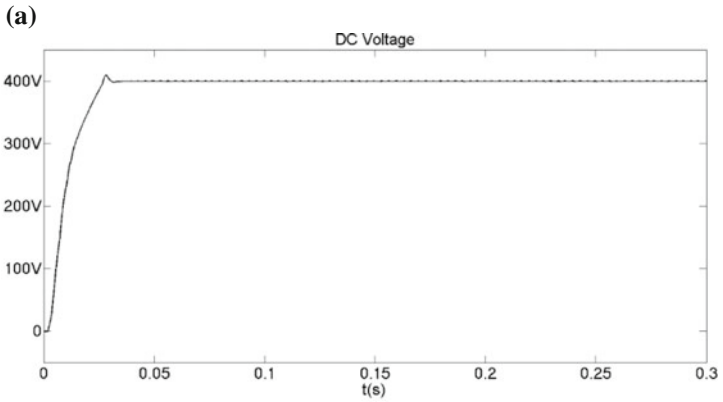
Since the switching state combination of the three-phase PWM rectifier is the same as that of the three-phase four-wire inverter, the specific implementation of 3-mode SVPWM and 4-mode SVPWM can be found in Chaps. 3 and 4, no more details will be described in this section.

9.3 Characteristic Analysis

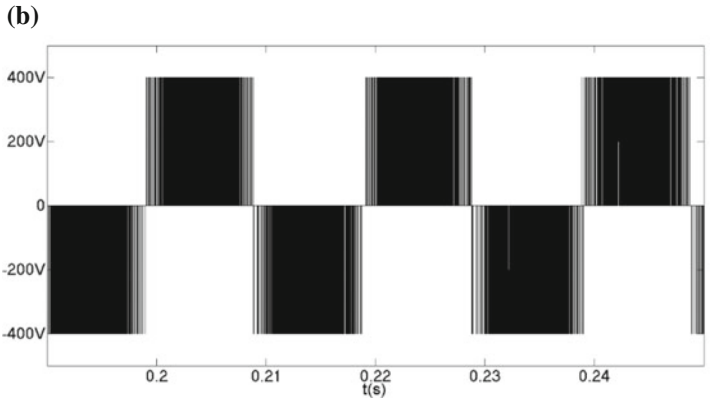
The output characteristics of a three-phase PWM rectifier under conventional SVPWM and *m*-mode SVPWM will be compared in this section. The simulation parameters are set as follows: RMS value of three-phase input voltage is 100 V, input frequency is 50 Hz, input inductance L is 5 mH, equivalent resistance r is 0.5 Ω, DC side capacitance C is 2250 uF, and switching frequency is 10 kHz. The control target is unity input power factor and the output DC voltage v_{dc} at 400 V.

9.3.1 Conventional SVPWM

The simulation results by using the conventional SVPWM are shown in Fig. 9.9. The output DC voltage in Fig. 9.9a can quickly reach the given reference voltage; The AC side voltage of the rectifier is shown in Fig. 9.9b; Fig. 9.9c shows that the input current is basically in phase with the AC power supply voltage; The harmonic contents of the input current is shown in Fig. 9.9d, and the total harmonic content (THD) is 3.57%.



Output DC voltage.

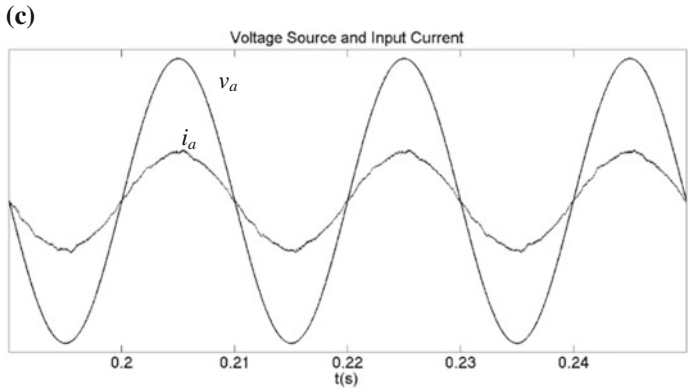


AC side voltage of the PWM rectifier.

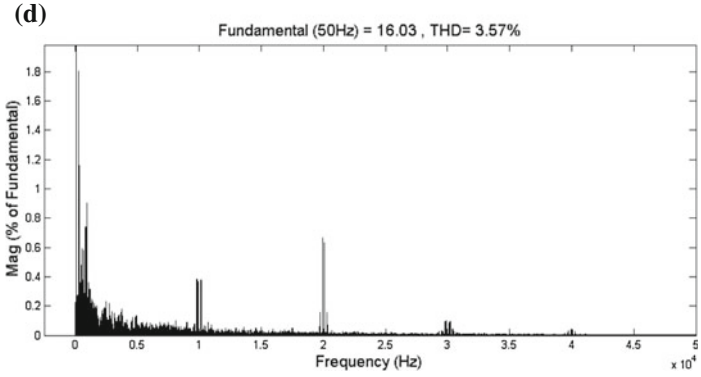
Fig. 9.9 Simulation results of conventional SVPWM

9.3.2 3-*Mode SVPWM*

Under the same simulation parameters, 3-mode SVPWM I and 3-mode SVPWM II were simulated, respectively, and the simulation results are shown in Figs. 9.10 and 9.11, respectively. It can be seen that the output DC voltages of 3-mode SVPWMs need a longer time to reach stable and the overshoot is larger, compared with the conventional SVPWM. The AC side voltage of the rectifier is greatly different from that of the conventional SVPWM, because the number of operating modes used in 3-mode SVPWM is reduced to half of those in conventional SVPWM. The input current under 3-mode SVPWM is still in phase with the AC power supply voltage, but has a higher THD than conventional SVPWM.



AC power supply voltage and input current.



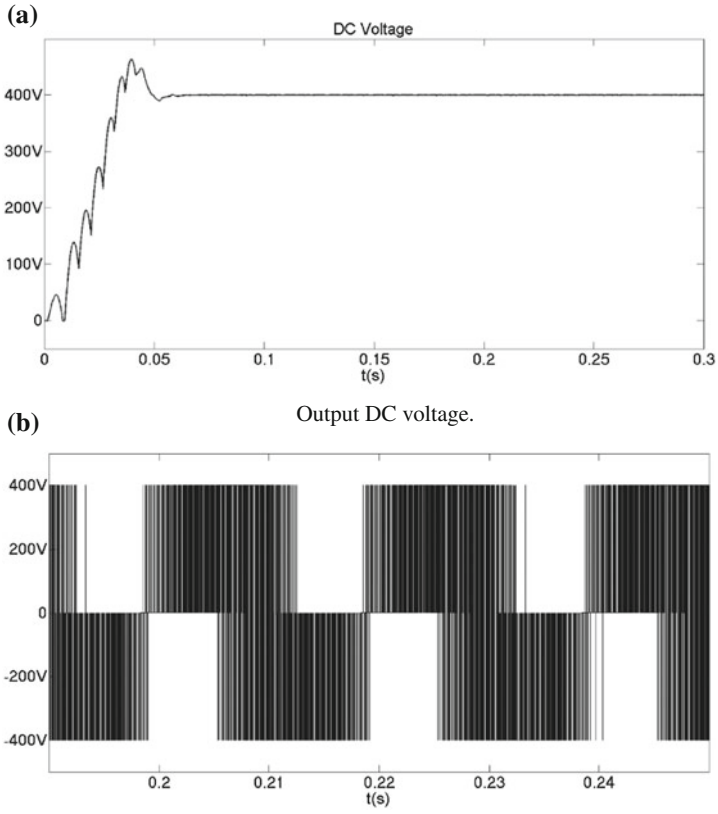
Harmonic contents of input current.

Fig. 9.9 (continued)

9.3.3 4-*Mode SVPWM*

When using the 4-mode SVPWM strategy, since one more voltage space vector is used than the 3-mode SVPWM, the rectifier can be modulated under the conventional SVPWM in partial sectors of the complex plane.

The simulation results of 4-mode SVPWMs I, II, and III are shown in Figs. 9.12, 9.13 and 9.14, respectively. Compared with the simulation results of 3-mode SVPWM, it is found that the transition process of output DC voltage is shortened and the overshoot is reduced, which is close to the control effect of conventional SVPWM. In addition, the AC side voltages of the PWM rectifier using 4-mode SVPWM I and II are basically the same as that of the conventional SVPWM, but that using 4-mode SVPWM III is still quite different from the conventional SVPWM. Furthermore, regardless which type of the 4-mode SVPWM strategy, the input current is in phase with the AC power supply voltage, and THD of the input current is



Output DC voltage.

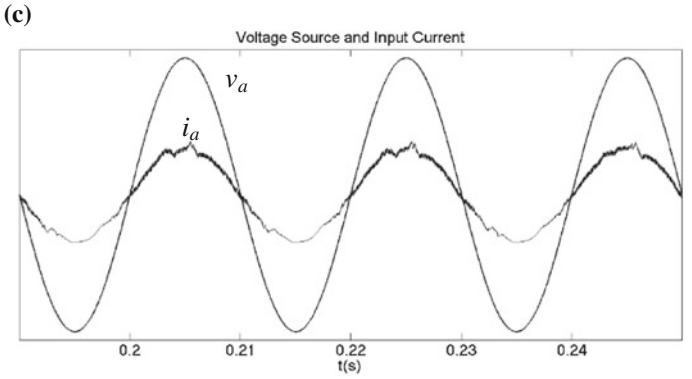
AC side voltage of the PWM rectifier.

Fig. 9.10 Simulation results of 3-mode SVPWM I

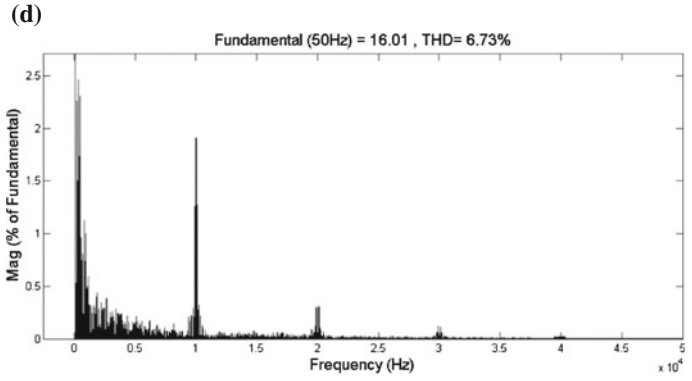
lower than that of 3-mode SVPWM, where THD of 4-mode SVPWM II is close to that of the conventional SVPWM.

9.4 Summary

In this chapter, based on the establishment of the switched linear system model, the state controllability of the three-phase voltage-source PWM rectifier has been proved. Referring to the conclusions of Chap. 2, the 3-mode and 4-mode controllability of the three-phase PWM rectifier have been discussed and the corresponding SVPWM strategies have been put forward. The simulation analysis and comparison of the proposed 3-mode SVPWM and 4-mode SVPWM strategies show that the *m*-mode SVPWM method is not only suitable for inverters, but also for voltage-source PWM rectifiers, which lays the foundation for the popularization and application of *m*-mode SVPWM.

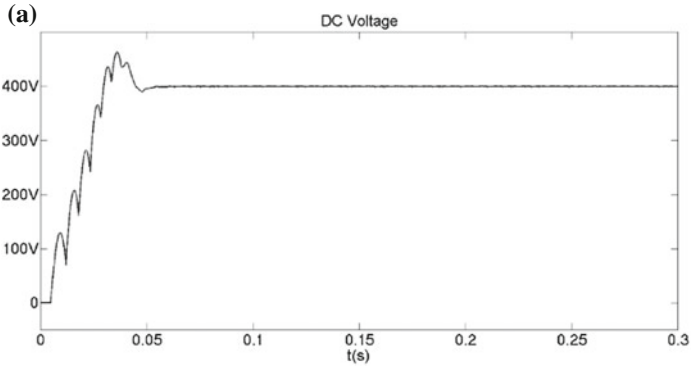


AC power supply voltage and input current.



Harmonic contents of input current.

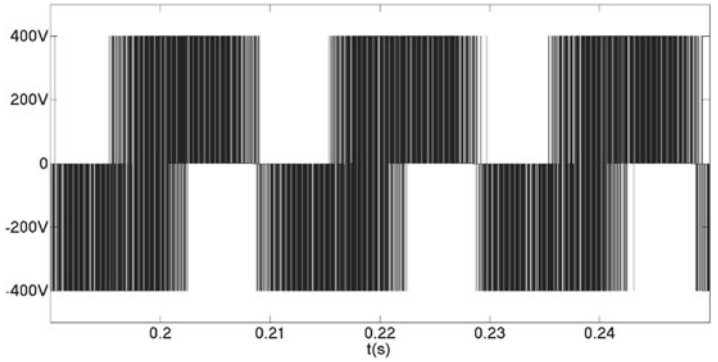
Fig. 9.10 (continued)



Output DC voltage.

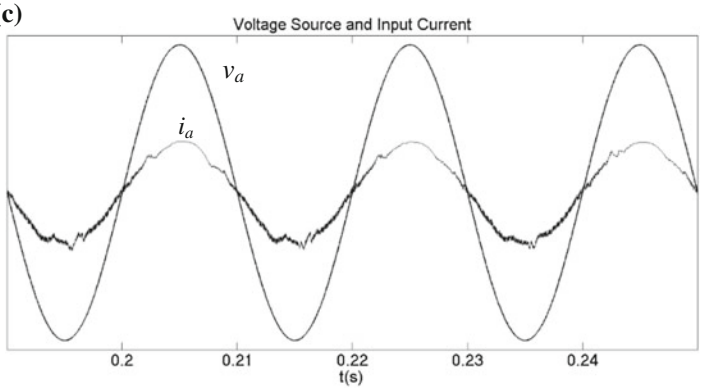
Fig. 9.11 Simulation results of 3-mode SVPWM II

(b)



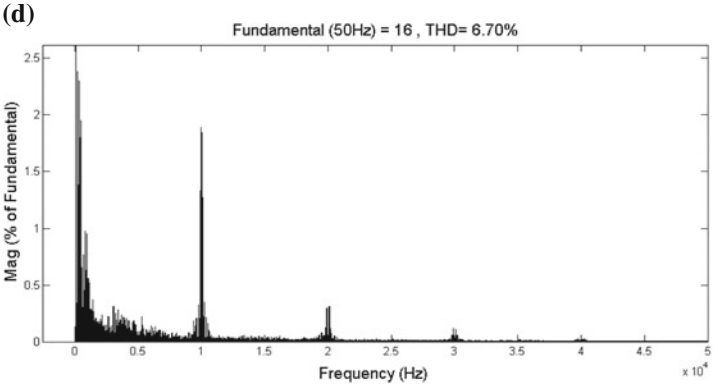
AC side voltage of the rectifier.

(c)



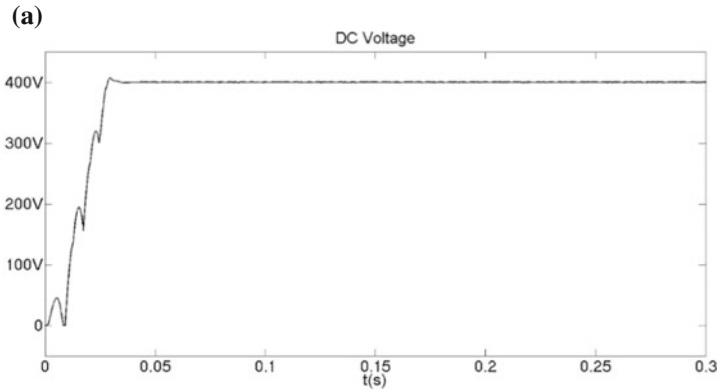
AC power supply voltage and input current.

(d)

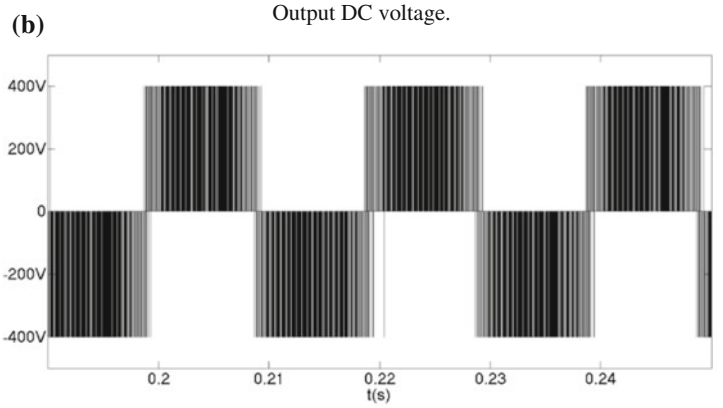


Harmonic contents of input current.

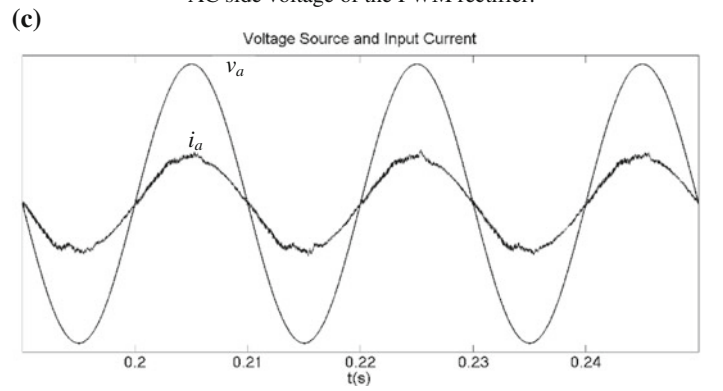
Fig. 9.11 (continued)



Output DC voltage.

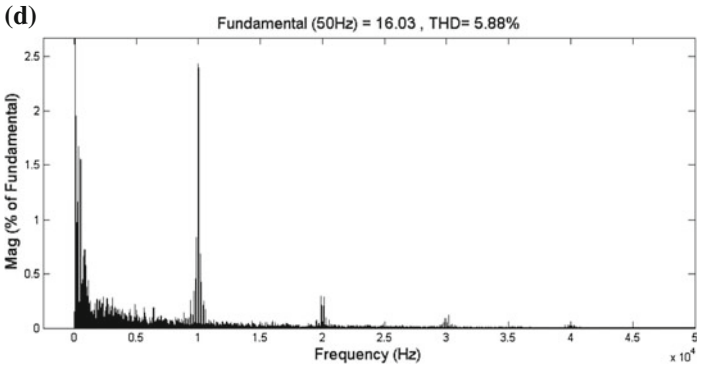


AC side voltage of the PWM rectifier.



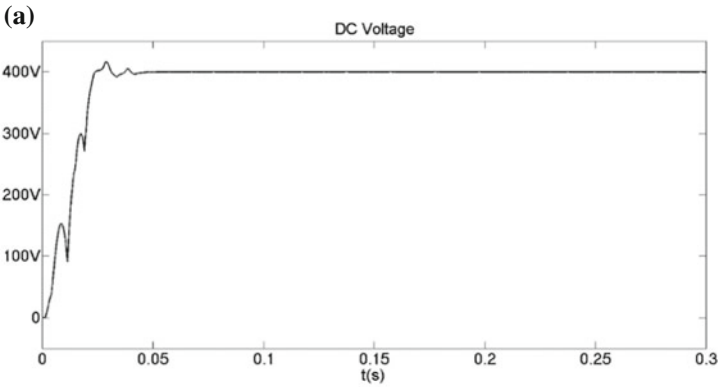
AC power supply voltage and input current.

Fig. 9.12 Simulation results of 4-mode SVPWM I

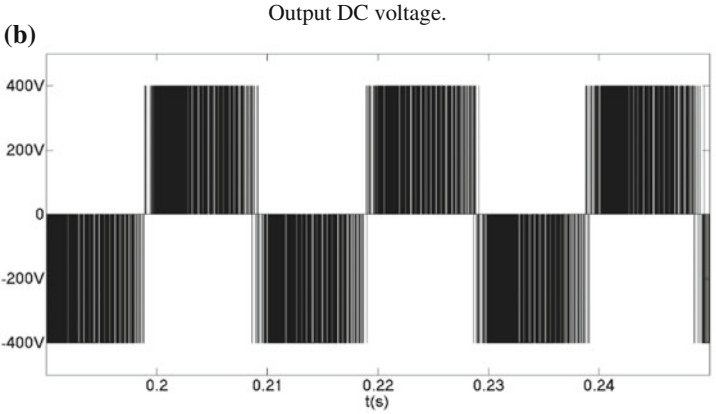


Harmonic contents of input current.

Fig. 9.12 (continued)

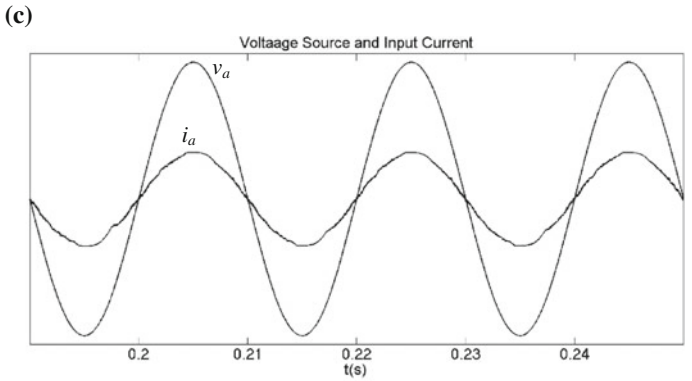


Output DC voltage.

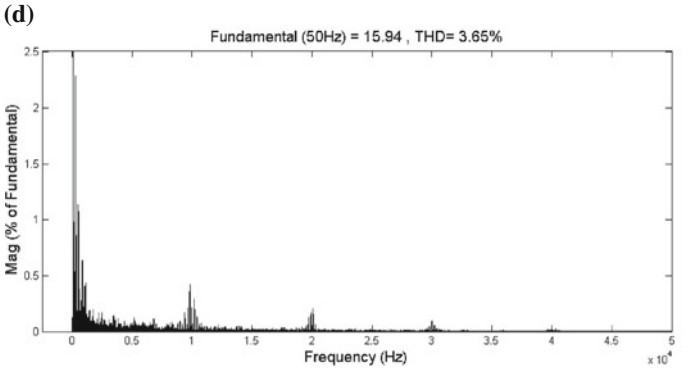


AC side voltage of the PWM rectifier.

Fig. 9.13 Simulation results of 4-mode SVPWM II

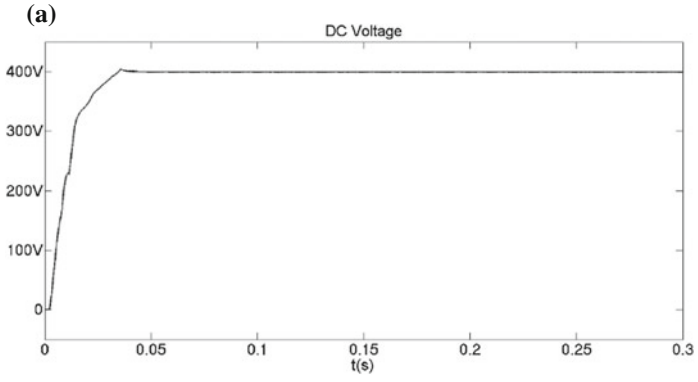


AC power supply voltage and input current.



Harmonic contents of input current.

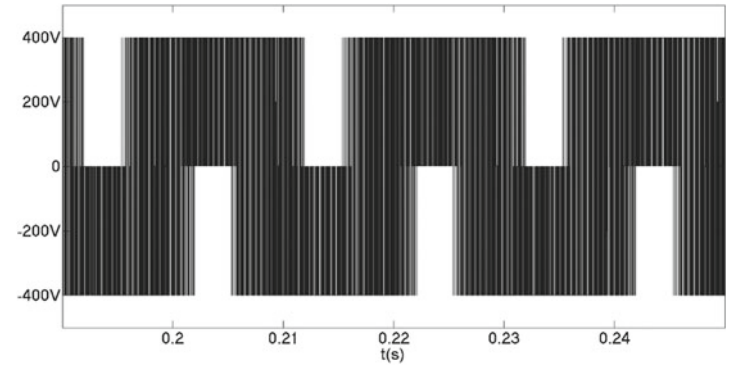
Fig. 9.13 (continued)



Output DC voltage.

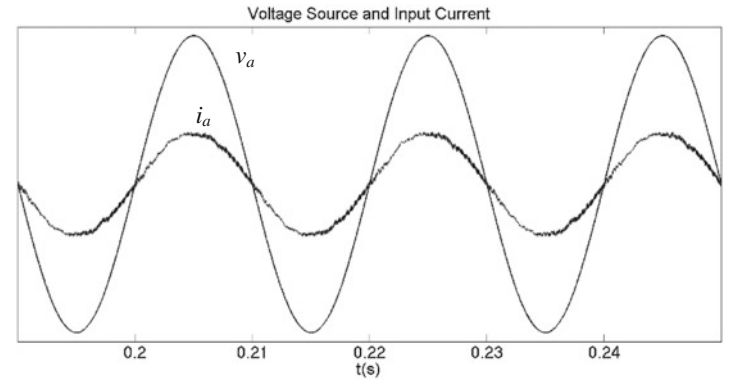
Fig. 9.14 Simulation results of 4-mode SVPWM III

(b)



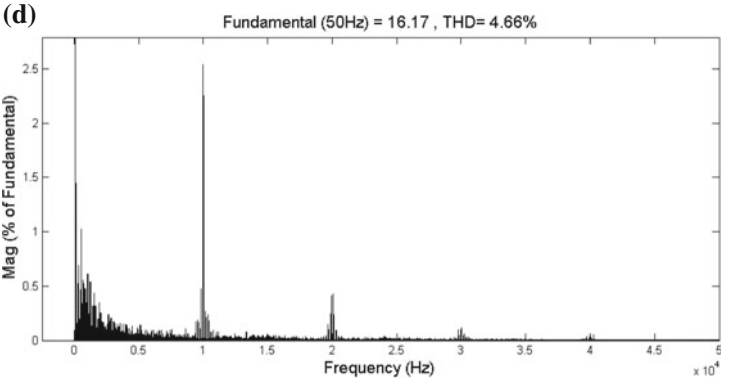
AC side voltage of the PWM rectifier.

(c)



AC power supply voltage and input current.

(d)



Harmonic contents of input current.

Fig. 9.14 (continued)

References

1. Kataoka T, Mizumachi K, Miyairi S (1979) A pulsewidth controlled ac-to-dc converter to improve power factor and waveform of ac line current. IEEE Trans Ind Appl 15(6):670–675
2. Busse A, Holtz J (1982) Multiloop control of a unity power factor fast switching ac to dc converter. In: IEEE Power electronics specialists conference, pp 171–179